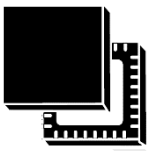
SPD1121 Datasheet

32-bit ARM® Cortex-M4 based MCU with 8-channel PWM, 7-channel 13-bit ADC and DPGA with comparator,integrated 3-phase 600V pre-driver

Features

- 32-bit ARM® Cortex-M4F CPU with FPU
  - Single precision floating-point unit (FPU)
  - 125 MHz maximum frequency
- Memories
  - Up to 128 KB flash (optional ECC protection), support XIP
  - 16 KB RAM (even parity protection)
- Reset and power management
  - 11~25 V single power supply
  - Built-in buck switching power supply, including over-temperature detection
  - Support VDDG overvoltage fault declaration
  - Support power-on reset POR and undervoltage/overvoltage detection BOD
- Clock
  - External clock access
  - Built-in 32MHz factory calibrated oscillator
  - Built-in 32MHz safe backup oscillator
  - Built-in phase locked loop (PLL) clock
- 13-bit A/D converter (up to 7 channels)
  - Minimum 250 ns conversion time
  - 2 differential sample-and-hold circuits
  - Analog signal input range: 0 ~ 3.339V
  - Support external input open and short circuit detection
  - 8 transition control channels
  - Supports transition priority control
  - Multiple event-triggered sampling transition requests
- Differential programmable gain amplifier (DPGA)
  - Programmable gain range: 2, 4, 8, 16, 24, 32, 48, 64



QFN38 (8 x 8 mm)

  - Setup time: 250 ns to 1.4 us
- 3 Analog comparators
  - Output with digital filter
  - 3 DAC reference sources
  - Can be used for overcurrent detection and phase comparison
- 4 Pulse Width Modulation Module (PWM)
  - 8 flexible configurable waveform outputs
  - Dedicated 16-bit timer
  - Support programmable phase control
  - Supports per-cycle or one-shot blocking Settings
  - Comparator outputs and blocking inputs can generate events or block trigger conditions.
  - All events can trigger CPU interrupts and ADC conversion request.
- Integrated three-phase 600V pre-driver
  - 200mA soucing current / 350mA sink current capability
  - Integrated 600V bootstrap diode
  - Built-in 400ns dead zone
  - Propagation delay matching for all channels
  - Each phase supports undervoltage protection (output low)
- 1 24-bit system tick timer
- 2 32-bit watchdog timers
- 2 32-bit general-purpose timers
- Up to 14 generic input-output pins

  - Independent pull-up/pull-down configuration
  - Independent output drive strength configuration
  - Independent input filter enable configuration
  - 7 multiplexable as analog inputs
- Enhanced Capture Module (ECAP)
  - Optional capture input pin
  - 4 32-bit capture registers
  - Optional capture or APWM mode
- Communication interface
  - UART×1, SPI×1, I2C×1
- Security module
  - CRC×1, 64-bit unique device identification number
- Debug mode
  - SWD
- Operating temperature
  - Junction temperature: -40 to +125°C.
  - Ambient temperature: -40 to +105°C.

Peripheral	SPD1121API38	SPD1121HAPI38
CPU maximum frequency (MHz)	125	
Flash (KB)	64	128
OTP Flash (Byte)	512	
SRAM (KB)	16	
GPIO	14	
13-bit ADC number of channel	1 7	
DPGA	1	
COMP	3	
DAC	3	
PWM number of channel	4 8	
ECAP	1	
GPT	2	
WDT	2	
CRC	1	
UART	1	
SPI	1	
I2C	1	

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Revision history

Version	Date	Author	Status	Changes
C/0	2025-02-26	J. Zhou	Outdated	1. Initial released.
C/1	2025-05-08	J. Zhou	Outdated	1. Modify description of features. 2. Modify Figure 1-2. 3. Modify description in Section 2.2, 2.7, 2.23. 4. Modify chapter sequence. 5. Modify Table 3-2. 6. Modify Table 3-5. 7. Modify Figure 5-1, Figure 5-2.
C/2	2025-07-03	J. Zhou	Outdated	1. Change the signal name of pin 10 to VCAP12A and the signal name of pin 30 to VCAP12B; rename the high-voltage pins. 2. Modify Figure 3-1. 3. Add the definition of the power-up slope for DVDD and VDDG in Table 5-2. 4. Add $\sum I_{OH}$ and $\sum I_{OL}$ in Table 5-3. 5. Modify the power supply range to 11~20V. 6. Modify the dead time of the pre-driver section to 400 ns. 7. Modify Table 5-1, Table 5-5. 8. Modify Figure 1-1, Figure 1-3.
C/3	2025-08-07	J. Zhou	Outdated	1. Modify Slew Rate During Power-up for VDDG in Table 5-2. 2. Modify f_{RCO} and add ACC_{RCO} in Table 5-9. 3. Modify Table 5-18 and Table 5-19.
C/4	2025-09-04	J. Zhou	Released	1. Add Figure 5-11. 2. Modify $C_{load(ext)}$ in Table 5-7. 3. Modify Table 5-11, add ADC performance under different frequency and clock source. 4. Modify Table 5-2. 5. Modify Table 5-17.

Terms or abbreviations

Terms or abbreviations	Description
MCU	Microcontroller Unit
LDO	Low Dropout Regulator
ECC	Error Correction Code

1 Device overview

SPD1121 is a highly integrated System-on-Chip (SoC) microcontroller featuring a 32-bit high-performance ARM® Cortex-M4 core. It offers a software-programmable clock frequency of up to 125MHz, 128KB of embedded FLASH, 16KB SRAM and a rich set of enhanced I/O and peripheral resources. It supports a 13-bit ADC, one differential programmable gain amplifier, four enhanced PWM modules, two general-purpose 32-bit timers, and communication interfaces such as UART, I2C, and SPI. Additionally, SPD1121 integrates a 3-phase pre-driver capable of handling 600V, designed to drive external MOSFETs or IGBTs. The pre-driver includes three 600V bootstrap diodes to save on-board components. All six pre-driver channels feature under-voltage lockout (UVLO). Overvoltage and overtemperature protections for VDDG are also integrated into the DC_DC power section, making it an ideal platform for motor control applications.

SPD1121 comes with a built-in switching power supply that supports an input range of 11~25V to generate a 3.3V power supply, and it also supports direct 3.3V external power supply. The operating temperature range is from -40°C to +125°C, and it is available in a 38-pin QFN package.

Figure 1-1 shows the application diagram for the SPD1121. Figure 1-2 shows the functional diagram. Figure 1-3 shows the clock tree information.

Figure 1-1: SPD1121 application diagram

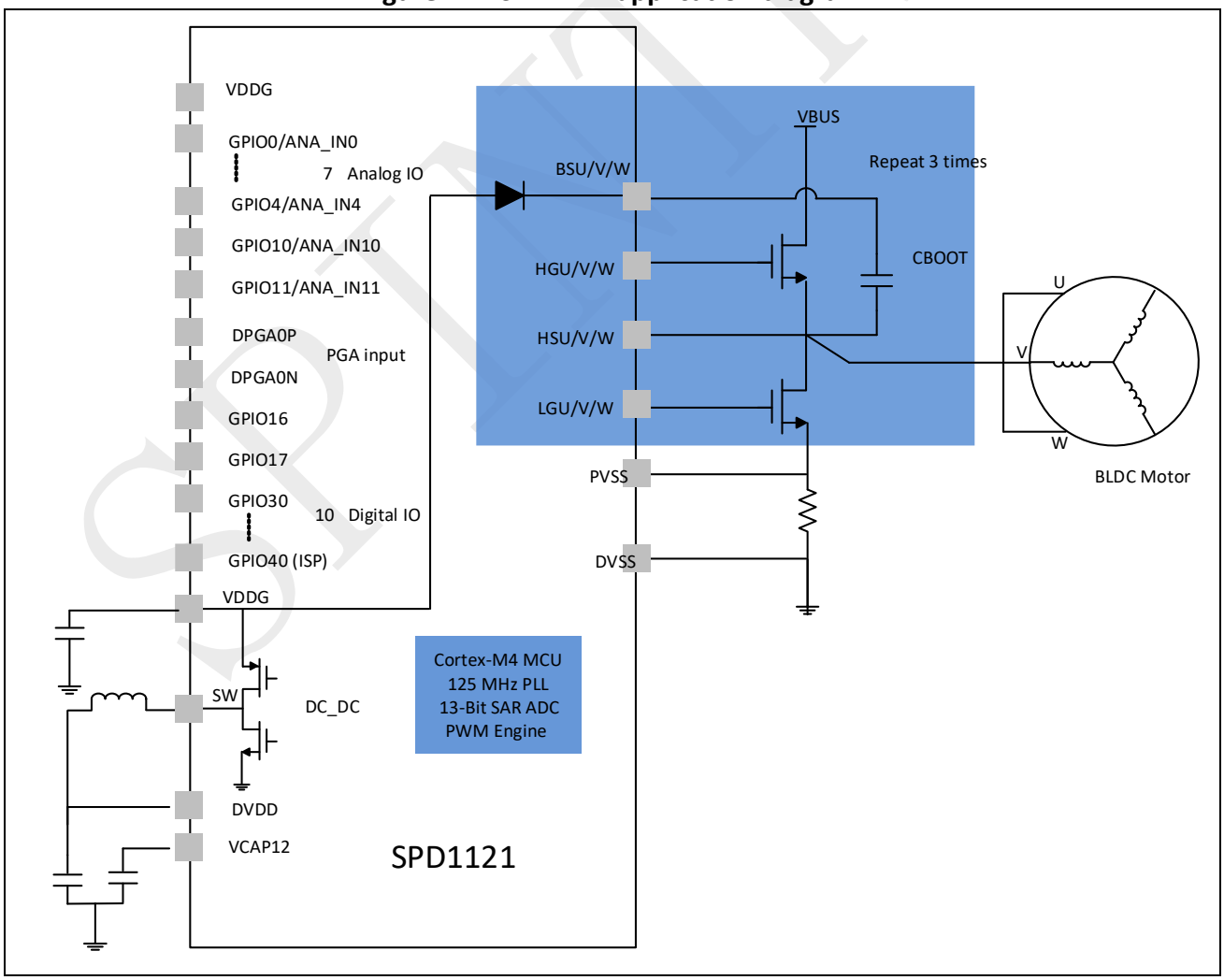


Figure 1-2: SPD1121 functional diagram

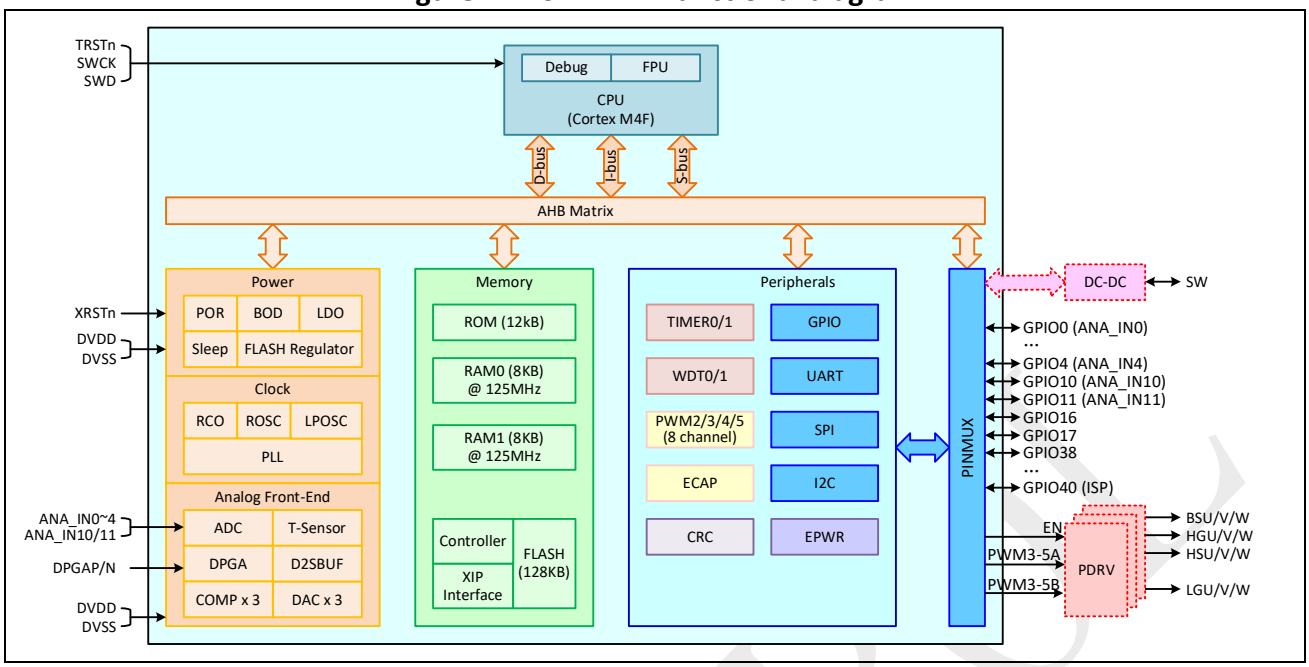
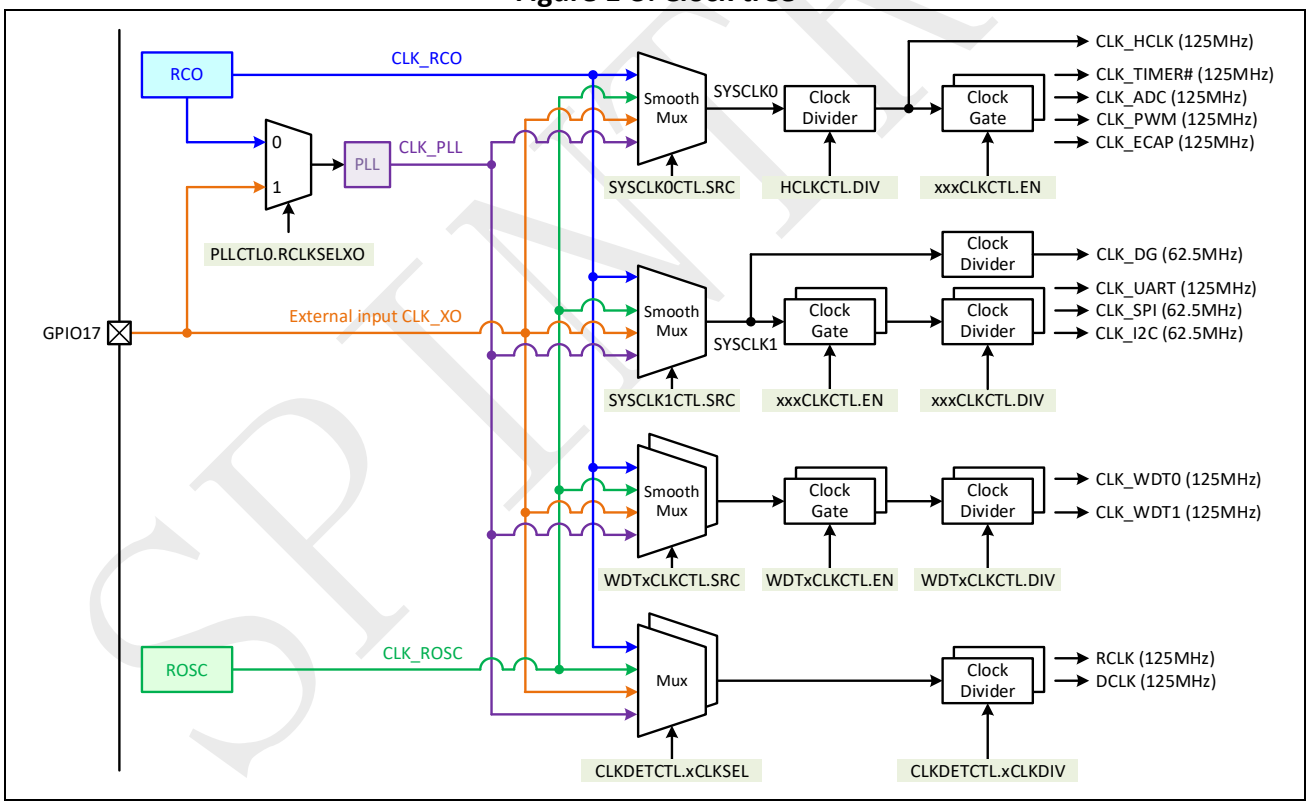


Figure 1-3: Clock tree



2 Feature descriptions

2.1 ARM® Cortex-M4F core

The ARM® Cortex-M4 processor is a cost-effective platform suitable for microprocessor designs that require high computational performance, fast interrupt response, low power consumption, and a compact pin count.

SPD1121 integrates a fully functional ARM® Cortex-M4 core with a Floating Point Unit (FPU), offering a maximum clock speed of 125MHz. It is compatible with all ARM® tools and software, making it a versatile choice for a wide range of applications.

2.2 Debug Interface

When the TRSTn pin is low, GPIO38 ~ GPIO40 are used for functions configured by user software. When the TRSTn pin is high, GPIO38 serves as SWD, GPIO39 as SWCK, and GPIO40 can be used as SWV.

When the underlying implementation of printf is achieved via ITM (Instrumentation Trace Macrocell) and GPIO40 is set to SWV (Serial Wire Viewer) mode, the corresponding signal can be observed on GPIO40 each time printf is called.

To use the SWV function, the MUXSEL field of PINMUX->GPIO40 must be configured to 6, and bit 24 of the ARM® Cortex-M4F register at address 0xE000EDFC (CoreDebug->DEMCR) must be set to 1.

2.3 Embedded SRAM

SPD1121 provides 16KB of on-chip RAM for storing code and data, supporting zero-wait-state read/write operations at up to 125MHz. It is divided into two 8KB partitions as follows:

- RAM0: Accessible via addresses 0x1FFFC000–0x1FFFDFFF or 0x20000000–0x20001FFF.
- RAM1: Accessible via addresses 0x1FFFE000–0x1FFFFFFF or 0x20002000–0x20003FFF.

All RAM supports even parity protection. A parity error can be configured to trigger either a reset or an interrupt. The address where the error occurred is recorded in the RAM0ERRADDR and RAM1ERRADDR registers for diagnostics.

2.4 Embedded Flash memory

SPD1121 features embedded Flash memory, offering up to 128KB of space for storing code and data. As shown in Figure 4-1, the Flash memory can be accessed via bus registers, and the state machine sends commands to erase or write to the Flash memory. It also supports reading the contents of the Flash memory through a specially designed Execute-In-Place (XIP) interface. Therefore, when SPD1121 starts up, the code in the Flash memory can be executed directly in place or loaded into RAM for execution in RAM.

For data security, the Flash memory provides ECC (Error Correction Code) functionality, which can correct single-bit errors and detect multi-bit errors. ECC errors can be configured to trigger either a reset or an interrupt. The address where the ECC error occured is recorded in the FLASHERRADDR register for diagnostics.

2.5 Nested vectored interrupt controller (NVIC)

The SPD1121 embeds a nested vectored interrupt controller able to handle up to 29 mask-able interrupt channels (not including the 16 interrupt lines of Cortex-M4F) and 16 programmable priority levels.

- Tightly Coupled NVIC enables faster interrupt response;
- Directly passes the interrupt vector table address to the core;
- Handles late-arriving but higher-priority interrupts;
- Supports interrupt tail-biting;
- Automatically saves the processor state;
- Automatically restores the context upon exiting the interrupt, eliminating the need for instruction overhead.

2.6 External interrupt/event controller(EXTI)

The SPD1121 provides a flexible external pin interrupt/event trigger mechanism. Any GPIO pin can be programmed as an external interrupt or event trigger source, offering one level-triggered interrupt and one edge-triggered interrupt.

2.7 Buck Switching Power Supply (DC-DC)

SPD1121 integrates a buck DC-DC converter with the following features:

- Provides 3.3V power for both the chip itself and other onboard circuits, with a recommended current capability of 200mA.
- The switching frequency can be configured to 400 kHz, 600 kHz, 1.2 MHz, or 2.4 MHz, featuring built-in spread spectrum modulation for improved EMI performance.
- Supports automatic PWM/PFM mode switching under light loads for higher efficiency.
- Offers forced PWM mode for minimal output ripple.
- Valley current limit is set at 400mA. If overloaded, the 3.3V output voltage will drop.
- Triggers an EPWRTZ signal upon detecting VDDG overvoltage, VDDG undervoltage, or pre-driver overtemperature.
- Supports disabling the internal DC-DC and switching to an external 3.3V power supply, with a required slew rate of less than 0.015 V/µs during power-up.
- Includes a global reset pin and Power-On Reset (POR) circuit, ensuring reliable power-up sequencing for simplified system design.

2.8 Brown-Out/Over voltage detection (BOD)

SPD1121 integrated Brown-Out/Over voltage detection (BOD).

The MCU section monitors the 3.3V/1.2V power domains and compares them against preset thresholds. When the voltage exceeds or falls below these thresholds, the system generates either an interrupt or a reset. The interrupt service routine then produces a warning message and transitions the microcontroller to a safe state. The brown-out/overvoltage detection feature can be enabled via software.

For the pre-driver section, it detects VDDG undervoltage conditions. When such condition occurs, the pre-driver outputs are forced to low level.

2.9 Clock

Upon power-up, the SPD1121 defaults to using the factory-calibrated 32MHz internal oscillator as its clock source. Users can switch to either an external clock or PLL clock via software configuration. The built-in PLL can select either an external clock or a 32 MHz internal oscillator as the input reference to generate clock signals ranging from 25 to 125 MHz.

As shown in Figure 1-3, a flexible clock tree can be achieved through clock source selection, enable control and frequency division control.

2.10 Boot mode

After SPD1121 is reset, the bootloader program located in ROM is executed and supports two boot modes as shown in Table 2-1:

- After power-on reset or XRSTn pin reset, if GPIO40 is detected low during startup, the system enters ISP boot mode. The bootloader will reprogram Flash or RAM via UART. During this process, GPIO34 is configured as UART_TXD function and GPIO35 is configured as UART_RXD function.
- In all other cases, the system enters normal boot mode, and the bootloader jumps to the starting address of Flash to begin execution.

Table 2-1: Boot mode

GPIO40	Reason for reset	Startup mode
0	Power-On Reset	ISP Mode: Reprogramme Flash or RAM via UART
0	XRSTn Reset	
0	ARM® CPU System Reset Request	Normal boot mode: Run the program from Flash memory
0	Power Overvoltage/Undervoltage	
0	PLL Loss of Lock/Clock Detection Circuit Error	
0	ROM/RAM/Flash Memory Error	
0	Watchdog Timer Timeout	
1	Any Reset	

2.11 General-purpose IOs (GPIOs)

SPD1121 provides 14 general-purpose input and output pins. Each pin can be configured by software for input, output, or peripheral multiplexing functions with the following characteristics:

- Each I/O pin includes configurable built-in pull-up and pull-down resistors.
- Each I/O pin features an enableable digital input filter.
- Each I/O pin can be configured as an external interrupt or event trigger source, with configurable active-level or edge triggering.

2.12 General-Purpose Timers

The SPD1121 provides two general-purpose timers with the following features:

- Independently configurable module clock enable control, with maximum clock frequency equal to the CPU frequency
- 32-bit auto-reload down counter
- Configurable to generate interrupts, ADC sampling conversion request events, or PWMSYNC events when the counter decrements to zero
- Supports three operating modes:
  - General timer mode: Periodic down-counting
  - Gated timer mode: External pin level enables counting
  - Event counter mode: Down-counting on external pin edge events

2.13 Watchdog Timer

The SPD1121 provides two watchdog timers with the following characteristics:

- Independent configuration of clock source, frequency division, and enable control, with maximum frequency equal to CPU frequency
- 32-bit auto-reload down counter
- Generates an interrupt when the counter decrements to zero
- Generates a reset when the counter decrements to zero and the interrupt flag is set
- In debug mode, the watchdog counter can be either frozen or allowed to run freely

2.14 System Tick Timer

The ARM® Cortex-M4F integrates one system tick timer, specifically designed for operating system use but also available as a standard down-counting timer. Its features include:

- 24-bit down counter
- Auto-reload capability
- Generates maskable system interrupt upon counter underflow

2.15 UART

SPD1121 supports 1 UART module with the following features:

- Independently configurable module clock enable control with maximum frequency equal to CPU frequency
- Capable of adding/removing standard asynchronous communication bits (start, stop, and parity) in serial data
- Configurable data length: 5 to 8 bits
- Supports multiple parity options: odd, even, forced high, forced low, or none
- Programmable stop bits: 1, 1.5, or 2 stop bits
- Maximum baud rate up to 1/16 of the clock frequency
- Automatic baud rate detection capability
- 64-byte FIFO for both transmit and receive channels

2.16 SPI

SPD1121 includes one SPI module. It features:

- Module clock enable and frequency division control are independently configurable, with a maximum frequency of 62.5MHz.
- Supports serial clock rates up to 30MHz, enabling communication speeds up to 30 Mbps.
- Operates in either master or slave mode.
- Flexible 1- to 32-bit programmable frame length.
- MSB-first (Most Significant Bit) data transmission order.
- Programmable clock polarity and phase control.
- 16×32-bit FIFO buffers for both transmit and receive paths.

2.17 I^2C

The I^2C bus interface complies with the common I^2C protocol. It features:

- Independent clock enable and prescaler control with maximum frequency of 62.5MHz
- Three speed modes:
  - Standard mode (100 kbps)
  - Fast mode (400 kbps / 1 Mbps)
  - High-speed mode (3.4 Mbps)
- Master or slave operation
- 7-bit or 10-bit addressing
- 7-bit or 10-bit combined format transmission
- Clock stretching support
- Detection of abort condition
- 16-byte FIFO for both transmit and receive paths

2.18 ADC

SPD1121 supports a 13-bit high-speed analog-to-digital converter, which can be used in motor control scenarios such as current sampling. Its features are as follows:

- 13 bit resolution;
- Minimum 250 ns transition time;
- 2 differential sample-and-hold circuits;
- Analog signal input range: 0 ~ 3.339V;
- Built-in 1.2V reference voltage;
- Input can come from 7 external IO inputs, temperature sensor, internal power supply, programmable gain amplifier output, D2SBUF output;
- Support external input open and short circuit detection;
- The clock-enabled control of the digital logic is independently configurable, and the highest frequency is the same as the CPU frequency;
- 8 conversion control channels, trigger source, input signal, sampling and conversion time, automatic average sample number can be configured independently, and independent EOC events are generated after conversion;
- Support for transition priority control;
- The following event-triggered sampling transition requests are supported:
  - Software trigger;
  - EOC event triggering
  - PWM REQ signal;
  - TIMER REQ signal;
  - External pin requests.

Refer to Table 5-11 for more features of the ADC.

2.19 Temperature sensor

The SPD1121 integrates one temperature sensor with the following characteristics:

- Generates a temperature-linear voltage output, internally connected to ADC input channels
- Measurement resolution: 1.74°C per 13-bit ADC code
- Measurement accuracy: ±12°C
- Operating range: -40°C to +125°C

2.20 DPGA

SPD1121 integrates one differential programmable gain amplifier (DPGA) with the following features.

- Dedicated analog input pins:
  - DPGAP, DPGAN
- Programmable gain (G_{DPGA}):
  - 2, 4, 8, 16, 24, 32, 48, 64
- Differential input voltage: ±2.7V / G_{DPGA}
- Common-mode input voltage (G_{DPGA}=2) : -1.5V ~ 2V
- Setup time: 250 ns to 1.4 us
- The output can be directly connected to a 13-bit high-speed ADC.

Refer to Table 5-12 for more characteristics of the differentially programmable gain amplifier.

2.21 Analog comparators (COMP)

SPD1121 supports 3 high-speed comparators. When combined with the internal digital-to-analog converter (DAC) as the reference, it can be used to detect whether the input or output voltage of the programmable gain amplifier exceeds the range. It has 3 10-bit DACs built-in to generate static voltages as the thresholds for the comparators, but it does not guarantee the performance of generating waveforms by dynamically changing the code values.
For the specific details of channel selection of the comparators, please refer to Section 3.6.

- Rail-to-rail input
- Offset voltage less than 10mV
- 50 ns typical corresponding time
- Programmable hysteresis
- Output with digital filter
- Phase comparison
- Compare the upper and lower boundaries (threshold can be matched) to realize overcurrent detection, and the result can be used to trigger PWM TZ event
- The output voltage of the 10-bit DAC is: V_{DVDD} / 1024 x Code

Please see Table 5-15 and Table 5-16 for analog comparator and DAC characteristics.

2.22 PWM

The SPD1121 supports 4 PWM modules (8 output channels) capable of independently generating complex waveforms without CPU intervention. Key features include:

- Dedicated 16-bit timer with independent period/frequency control
- Dual outputs per module, supporting:
  - Single-edge operation
  - Dual-edge symmetric operation
  - Dual-edge asymmetric operation
- Event-triggered capabilities:
  - CPU interrupts
  - ADC conversion initiation
- Programmable phase control (lead/lag) relative to other PWM modules
- Dead-time generation with independent rise/fall edge delay control
- Protection modes:
  - Cycle-by-cycle or one-shot lockdown
  - Configurable forced output states during lockdown (high/low/high-Z)
- Trigger integration:
  - Comparator outputs and lockdown inputs can generate events or trigger protection conditions

2.23 Three-Phase Pre-Driver

The SPD1121 integrates 3 pairs of independent high/low-side drivers for driving external MOSFETs or IGBTs in three-phase control applications, with the following features:

- Sourcing/sinking capability: 200mA (pull-up) / 350mA (pull-down)
- Matched propagation delay across all 6 channels: 400ns (typical)
- PWM-configurable input waveform control
- Global enable control: Simultaneously disables all 6 pre-driver outputs when deactivated
- High-side floating voltage up to 600V for driving power MOSFET/IGBT high-side switches
- Built-in dead time: 400ns (typical) to prevent shoot-through
- Integrated noise filtering:
  - Pulses shorter than 250ns are filtered out
  - Pulses longer than 250ns pass through without pulse-width distortion

2.24 ECAP

The SPD1121 incorporates one ECAP module with the following characteristics:

- Flexible input capture pin selection: Any GPIO can be configured as a capture pin
- 32-bit timer-based counter
- Four 32-bit timestamp capture registers
- 4-level sequencer synchronized with external events
- Independent edge polarity selection (rising/falling edge) for all 4 events
- Interrupt support for all 4 events

2.25 Cyclic redundancy check (CRC)

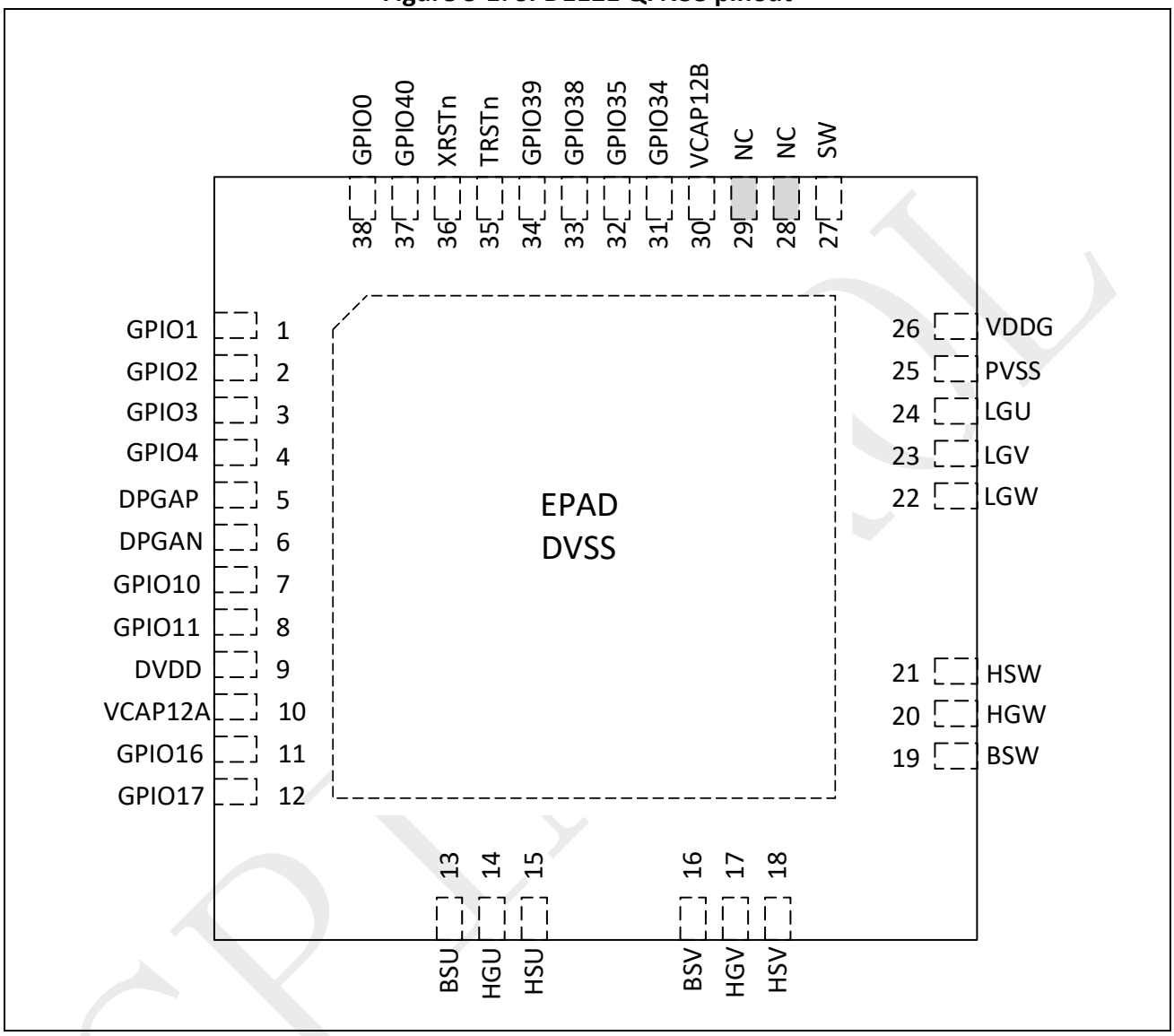
The SPD1121 integrates a dedicated hardware CRC unit for data transmission/storage integrity verification, featuring:

- 32-bit parallel data stream input
- Support up to 2^{32} bytes length for CRC calculation
- Support for 5 standard CRC polynomials

3 Pinout and pin description

3.1 QFN38

Figure 3-1: SPD1121 QFN38 pinout



[1] The figure above shows top view for the package.

[2] Note: when TRSTn is high, GPIO38 ~ GPIO39 may be used for debug interface, cannot be reconfigured for other functions.

Table 3-1: SPD1121 QFN38 pin definitions

Pin	Signal	Sub-Type[1]	Description
1	GPIO1	I/O	Universal input/output 1
	ANA_IN1	AI	ADC channel 1 input
	COMP0H	O	Comparator COMP0H result output
2	GPIO2	I/O	Universal input/output 2
	ANA_IN2	AI	ADC channel 2 input
	COMP1H	O	Comparator COMP1H result output
3	GPIO3	I/O	Universal input/output 3
	ANA_IN3	AI	ADC channel 3 input
	COMP0L	O	Comparator COMP0L result output
4	GPIO4	I/O	General purpose input/output 4
	ANA_IN4	AI	ADC channel 4 input
	COMP0H	O	Comparator COMP0H result output
5	DPGAP	AI	Programmable gain amplifier 0 positive input
6	DPGAN	AI	Programmable gain amplifier 0 negative input
7	GPIO10	I/O	General purpose input/output 4
	ANA_IN10	AI	ADC channel 4 input
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	COMP1H	O	Comparator COMP1H result output
8	GPIO11	I/O	Universal input/output 11
	ANA_IN11	AI	ADC channel 11 input
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	DCLK	O	CLKDET module monitor the clock output
	EPWRTZO	O	ePower module monitor the blockade signal output
	COMP0L	O	Comparator COMP0L result output
9	DVDD	S	Digital power supply, adding 10uF and 0.1uF to bypass ceramic capacitors to DVSS
10	VCAP12A	S	1.2V power supply with addition of 2.2uF and 0.1uF bypass ceramic capacitors to DVSS
11	GPIO16	I/O	Universal input/output 16
	PWM_SYNCO	O	PWM REQ monitor the signal output
	UART_RXD	I	UART receive the data
	UART_TXD	O	UART send the data
	PWM2A	O	PWM2 output A
	PWM5A	O	PWM5 output A
	SPI_SFRM	I/O	SPI chip selection signal
12	GPIO17	I/O	Universal input/output 17
	XIN	AI/I	External oscillator input
	UART_RXD	I	UART receive the data
	UART_TXD	O	UART send the data
	PWM2B	O	PWM2 output B
	PWM5B	O	PWM5 output B
	SPI_SCLK	I/O	SPI clock input/output

Pin	Signal	Sub-Type[1]	Description
13	BSU	S	Pre-driver U-phase bootstrap points, 4.7uF and 0.1uF of 50V ceramic chip capacitors to HSU
14	HGU	O	Pre-driver U phase upper tube gate drive
15	HSU	S	Pre-driver U-phase voltage drive
16	BSV	S	Pre-driver V phase bootstrap points, 4.7uF and 0.1uF of 50V ceramic chip capacitors to HSV
17	HGV	O	Pre-driver phase V upper tube gate drive
18	HSV	S	Pre-driver V phase voltage drive
19	BSW	S	Pre-driver W phase bootstrap points, 4.7uF and 0.1uF of 50V ceramic chip capacitors to HSW
20	HGW	O	Pre-driver W phase upper tube gate drive
21	HSW	S	Pre-driver W phase voltage drive
22	LGW	O	Pre-driver W phase lower tube gate drive
23	LGV	O	Pre-driver phase V lower tube gate drive
24	LGU	O	Pre-driver U phase lower tube gate drive
25	PVSS	S	Pre-driver field
26	VDDG	S	11 to 25V power input, add at least 2.2uF and 0.1uF bypass ceramic capacitors to DVSS
27	SW_DCDC	S	DC-DC switch node, add 10uH electrical sense DVDD. The saturation current of the inductor needs to be greater than 600mA.
28	NC	–	–
29	NC	–	–
30	VCAP12B	S	1.2V power supply with addition of 0.1uF bypass ceramic capacitors to DVSS
31	GPIO34	I/O	Universal input/output 34
	UART_TXD	O	UART send the data
	UART_RXD	I	UART receive the data
	I2C_SDA	I/O	I2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	I2C_SCL	I/O	I2C clock
32	GPIO35	I/O	Universal input/output 35
	UART_RXD	I	UART receive the data
	UART_TXD	O	UART send the data
	I2C_SCL	I/O	I2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	I2C_SDA	I/O	I2C data
33	GPIO38	I/O	Universal input/output 38
	SWD	I/O	SWD debug port data signal
	I2C_SDA	I/O	I2C data
	SPI_MOSI	I/O	SPI master output, slave input
	SPI_MISO	I/O	SPI master input, slave output
	PWM2A	O	PWM2 output A
	SPI_SCLK	I/O	SPI clock input/output

Pin	Signal	Sub-Type[1]	Description
	Note: When TRSTn is high, this pin is always used as SWD and cannot be configured for other functions.		
34	GPIO39	I/O	Universal input/output 39
	SWCK	I	SWD debug port clock signal
	I2C_SCL	I/O	I2C clock
	SPI_MISO	I/O	SPI master input, slave output
	SPI_MOSI	I/O	SPI master output, slave input
	PWM2B	O	PWM2 output B
	SPI_SFRM	I/O	SPI frame signal
	Note: When TRSTn is high, this pin is always used as SWCK and cannot be configured for other functions.		
35	TRSTn	I	The SWD reset the pin and reset the SWD when the level is low
36	XRSTn	I	Chip reset pin, low level valid
37	GPIO40 (ISP)	I/O	Universal input/output 40 (start mode selector pin)
	SPI_SCLK	I/O	SPI clock input and output
	UART_TXD	O	UART sends the data
	DCLK	O	CLKDET module monitor the clock output
	EPWRTZ0O	O	The blocking signal 0 used by the ePower module for monitoring
	EPWRTZ1O	O	The blockade signal 1 used by the ePower module for monitoring
	Note: When TRSTn is high, with the MUXSEL field of PINMUX->GPIO40 configured to 6, and bit 24 of the ARM® Cortex-M4F register at address 0xE000EDFC (CoreDebug->DEMCR) set to 1, this pin will permanently function as SWV and cannot be configured for any other purpose.		
38	GPIO0	I/O	Universal input/output 0
	ANA_IN0	AI	ADC channel 0 input
	COMP0L	O	Comparator COMP0L result output

[1] I = digital input, O = digital output, AI = analog input, AO = analog output, S = power supply.

[2] Any GPIO pin can be configured for ECAP input and output.

3.2 GPIO pin function and state after reset

Table 3-2: GPIO pin function and state after reset

Pin Name	Default Function	Default State
GPIO0	ADC0	Floating
GPIO1	ADC1	Floating
GPIO2	ADC2	Floating
GPIO3	ADC3	Floating
GPIO4	ADC4	Floating
GPIO10	ADC10	Floating
GPIO11	ADC11	Floating
GPIO16	GPIO16	Floating
GPIO17	GPIO17	Floating
GPIO18[1]	GPIO18	Pull down
GPIO19[1]	GPIO19	Pull down
GPIO20[1]	EPWR_TZ0I	Pull down
GPIO24[1]	GPIO24	Pull up
GPIO25[1]	EPWR_TZ0I	Floating
GPIO26[1]	GPIO26	Pull down
GPIO27[1]	GPIO27	Pull down
GPIO28[1]	GPIO28	Pull down
GPIO29[1]	GPIO29	Pull down
GPIO32[1]	GPIO32	Pull up
GPIO34	GPIO34	Pull up
GPIO35	GPIO35	Pull up
GPIO38	GPIO38	Floating
GPIO39	GPIO39	Floating
GPIO40	GPIO40 (ISP boot)	Pull up

[1] Internal pins.

3.3 Connection between the MCU and the pre-driver

Table 3-3: Connection between the MCU and the pre-driver

Pin	Configuration	Description of the pre-driver signal
GPIO20	GPIO output	Enable control of pre-driver
GPIO18	PWM3A	PWM waveform input at the upper end of the pre-driver W phase
GPIO19	PWM3B	PWM waveform input at the lower end of the pre-driver W phase
GPIO26	PWM4A	PWM waveform input at the upper end of the pre-driver V phase
GPIO27	PWM4B	PWM waveform input at the lower end of the pre-driver V phase
GPIO28	PWM5A	PWM waveform input at the upper end of the pre-driver U phase
GPIO29	PWM5B	PWM waveform input at the lower end of the pre-driver U phase

3.4 Connection relationship between MCU and DC-DC

Table 3-4: Connection relationship between MCU and DC-DC

Pin	Configuration	Description of the DC-DC signal
GPIO24	EPWRSDAT	DC-DC SPI data signal
GPIO25	EPWRSCLK	DC-DC SPI clock signal
GPIO32	EPWRSFRM	DC-DC SPI chip selection signal

3.5 ADC input channel selection

Table 3-5: ADC input channel selection

Option	SH0		SH1	
	SHINSELP	SHINSELN	SHINSELP	SHINSELN
0	GND		GND	
1	TSENSOR_P	TSENSOR_N	ATEST	DAC2
2	DPGA_OUTP	DPGA_OUTN	–	–
3	VDD33	DAC0	VDD12	DAC1
4	ANA_IN0	ANA_IN1	ANA_IN2	ANA_IN3
5	ANA_IN1	ANA_IN0	ANA_IN3	ANA_IN2
6	ANA_IN4	D2SBUF	ANA_IN4	–
7	ANA_IN10	ANA_IN11	ANA_IN10	ANA_IN11

3.6 Comparator input channel selection

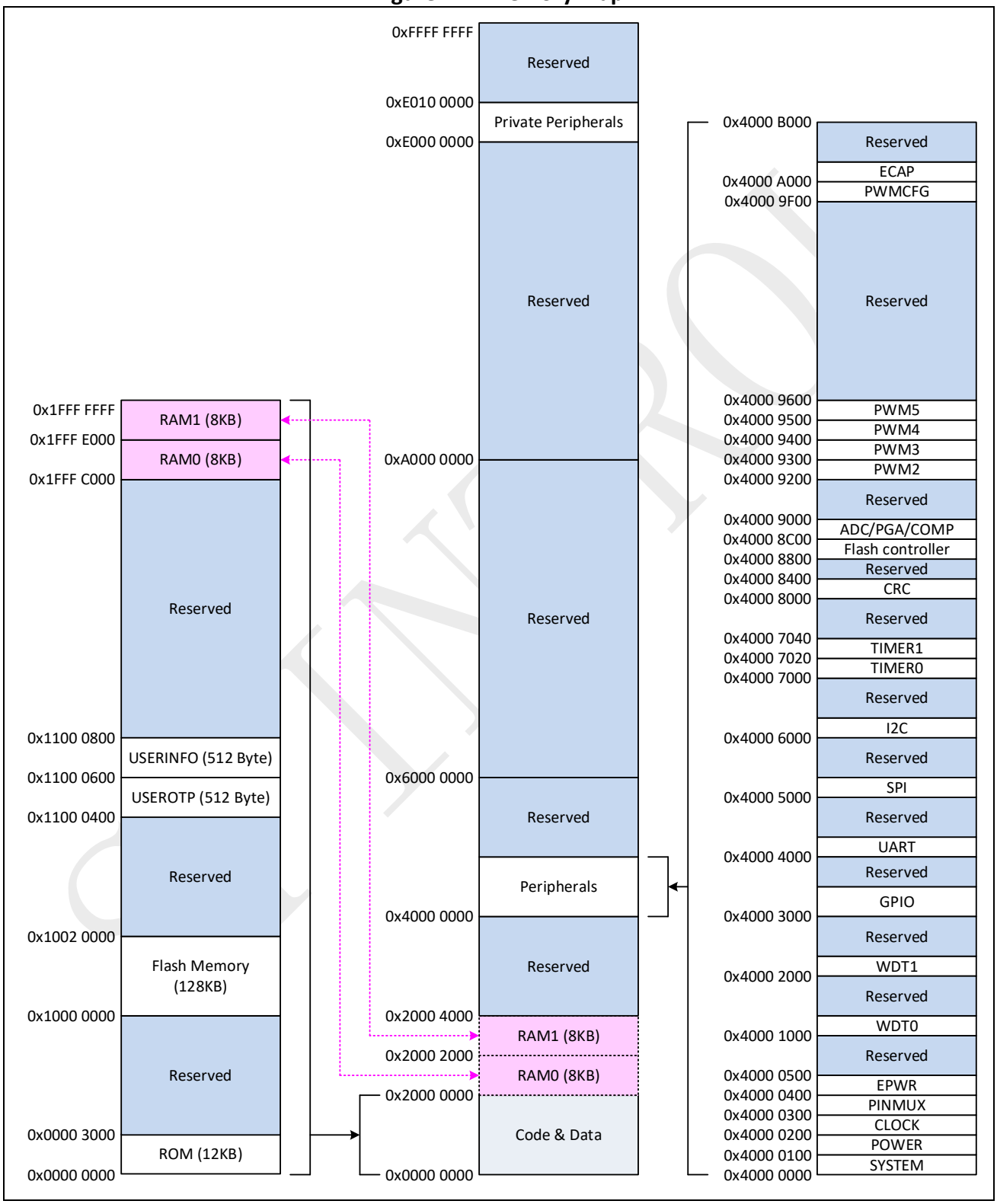
Table 3-6: Comparator input channel selection

INSEL	COMP0L		COMP0H		COMP1H	
	Input signal	Reference signal	Input signal	Reference signal	Input signal	Reference signal
0	D2SBUF	DAC1	D2SBUF	DAC0	D2SBUF	DAC2
1	–	DAC1	–	DAC0	–	DAC2
2	ANA_IN0	DAC1	ANA_IN0	DAC0	ANA_IN0	DAC2
3	ANA_IN1	DAC1	ANA_IN1	DAC0	ANA_IN1	DAC2
4	ANA_IN2	DAC1	ANA_IN2	DAC0	ANA_IN2	DAC2
5	ANA_IN3	DAC1	ANA_IN3	DAC0	ANA_IN3	DAC2
6	ANA_IN10	DAC1	ANA_IN10	DAC0	ANA_IN10	DAC2
7	ANA_IN11	DAC1	ANA_IN11	DAC0	ANA_IN11	DAC2

4 Memory mapping

The memory map of SPD1121 is shown in Figure 4-1.

Figure 4-1: Memory map



4.1 Boot ROM

SPD1121 is integrated with 12KB on-chip ROM for storing bootloader, function library related to system and Flash management and mathematical library commonly used in user code. It supports ECC protection and can correct single-bit error and detect multi-bit error. ECC errors can be configured to trigger reset or interrupts, and the address where the ECC error occurred is recorded in the ROMERRADDR register for diagnosis.

As shown in Figure 4-2, in order to facilitate users to perform system management, Flash operation and trigonometric functions and other operations, the function library is fixed in ROM, and the start address stored in the entry address vector table is 0x0000 2F60. Table 4-1 lists the library details.

To protect the code, the user is only allowed to read the contents of the entry address vector table and execute the function library code, but not the specific contents of the function.

Figure 4-2: ROM storage space partition

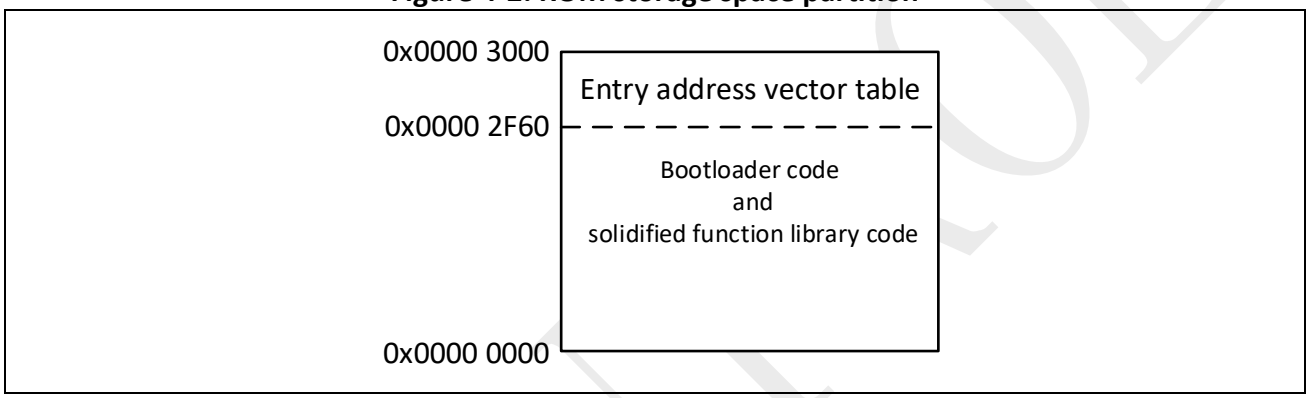


Table 4-1: Solidified library entry address vector table

Function name	Vector address	Descripton
FLASH_SetTiming	0x0000 2F60	Flash timing parameters are configured according to the clock frequency
FLASH_Init	0x0000 2F64	Initialize the Flash configuration
FLASH_Read	0x0000 2F68	Read Flash content (regular 0/1 threshold)
FLASH_VerifyProgramRead	0x0000 2F6C	Reading the Flash content is used to verify whether the burning is correct (Using a threshold that is more difficult to read to 0)
FLASH_VerifyEraseRead	0x0000 2F70	Reading the Flash content is used to verify that the erasure is correct (Adopt a threshold that is more difficult to read to 1)
FLASH_VerifyErase	0x0000 2F74	Check if the Flash in the specified area has been successfully erased
FLASH_Erase	0x0000 2F78	Erase the address specified by Flash in the specified way (this function is not open to customers)
FLASH_EraseSector	0x0000 2F7C	Erases the Flash sector specified
FLASH_EraseBlock	0x0000 2F80	Erases the block specified by Flash
FLASH_EraseChip	0x0000 2F84	Erase the Flash's entire primary partition

Function name	Vector address	Descripton
FLASH_ProgramWord	0x0000 2F88	Burn a word (32 bits) to the specified Flash address
FLASH_Program	0x0000 2F8C	Burn a set of data to Flash specified address
FLASH_WriteProtect	0x0000 2F90	Enable write protection of the specified area of the Flash primary partition
FLASH_WriteUnProtect	0x0000 2F94	Disable write protection for the specified region of the Flash primary partition
SYSTEM_Sleep	0x0000 2F98	Configure the wake-up condition and put the system into sleep mode
AtanF32	0x0000 2F9C	A library provided by the application team
ThetaRadWrap	0x0000 2FA0	
SAT0	0x0000 2FA4	
SVPWM	0x0000 2FA8	
ClarkeF32	0x0000 2FAC	
InvParkF32	0x0000 2FB0	
ParkF32	0x0000 2FB4	
BubbleSortForCurrent	0x0000 2FB8	
Motor_1PhaseCurrentReconstruct	0x0000 2FBC	
Motor_1PhaseCurrentSamplingShift	0x0000 2FC0	
arm_sin_f32	0x0000 2FC4	
arm_cos_f32	0x0000 2FC8	

5 Electrical characteristics

5.1 Absolute maximum ratings

Table 5-1: Absolute maximum ratings[1][2]

Symbol	Parameter	Min	Max	Unit
V_{VDDG}	Buck DC-DC supply voltage, relative to V_{DVSS}	-0.3	30	V
$I_{DC-DC(VALLY)}$	Buck output valley current	–	400	mA
V_{DVDD}	Supply voltage, relative to V_{DVSS}	-0.3	4.6	V
V_{IN}	Input voltage (V_{DVDD} = 3.3V)	-0.3	4.6	V
V_O	Output voltage	-0.3	4.6	V
I_{IC}	Input clamp current	-20	+20	mA
I_{OC}	Output clamp current	-20	+20	mA
V_{HS}	Phase voltage drive	V_{BS} - 30	V_{BS} + 0.3	V
V_{BS}	Upper tube bootstrap point voltage	-0.3	600	V
V_{HG}	Upper tube gate drive voltage	V_{HS} - 0.3	V_{BS} + 0.3	V
V_{LG}	Lower tube gate drive voltage	-0.3	V_{VDDG} + 0.3	V
SR_{HS}	Voltage swing rate allowed by VPX	–	50	V/ns
T_J	Junction temperature [3]	-40	+125	°C
T_A	Ambient temperature [3]	-40	+105	°C
T_{stg}	Storage Temperature [3]	-65	+150	°C

[1] Stresses outside the absolute maximum rating range may cause permanent damage to the device. These values are only rated stresses and do not imply that the device functions properly under these conditions.

[2] Unless otherwise stated, all voltages are based on V_{DVSS}.

[3] Long-term high temperature storage or use under maximum temperature conditions may reduce the lifetime of the device.

5.2 Recommended operating conditions

Table 5-2: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VDDG}	Digital supply voltage	–	11.0	15	25	V
V_{DVDD}	Analog supply voltage	–	2.97	3.3	3.63	V
dV_{VDDG}/dt	Slew Rate During Power-up for VDDG	–	–	–	TBD	V/ms
dV_{DVDD}/dt	Slew Rate During Power-up for Externally Supplied DVDD	–	–	–	0.015	V/us
I_{DC-DC}	DC-DC power supply capability	–	–	–	200	mA
V_{IH}	High level input voltage	V_{DVDD} = 3.3 V	2.0	–	V_{DVDD} + 0.3	V
I_{OH}	When $V_{OH} = V_{OH(MIN)}$, high level output, source current	STRENGTH = 0 STRENGTH = 1 STRENGTH = 2 STRENGTH = 3	–	–	4.5 9 13.5 18	mA
I_{OL}	When $V_{OL} = V_{OL(MAX)}$, low level output, perfusion current	STRENGTH = 0 STRENGTH = 1 STRENGTH = 2 STRENGTH = 3	–	–	4.5 9 13.5 18	mA
V_{HS}	Phase voltage drive	–	–	–	600	V
V_{BS}	Upper tube bootstrap point voltage	–	V_{HS} + 11	–	V_{HS} + 20	V
V_{HG}	Upper tube gate drive voltage	–	V_{HS}	–	V_{BS}	V
V_{LG}	Lower tube gate drive voltage	–	V_{PVSS}	–	V_{VDDG}	V
T_J[1]	Temperature of junction	–	-40	–	+125	°C
T_A	Ambient temperature	–	-40	–	+105	°C

[1] All properties were measured at T_J = -40 to +125 °C in subsequent sections unless otherwise noted.

5.3 I/O Electrical characteristics

Table 5-3: IO Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High level output voltage	$I_{OH} = I_{OH(MAX)}$	V_{DVDD} - 0.5	–	–	V
V_{OL}	Low output voltage	$I_{OL} = I_{OL(MAX)}$	–	–	0.4	V
V_{IH}	High level input voltage	V_{DVDD} = 3.3 V	2.0	–	V_{DVDD} + 0.3	V
V_{IL}	Low input voltage	V_{DVDD} = 3.3 V	V_{DVSS} - 0.3	–	0.8	V
I_{OH}	When $V_{OH} = V_{OH(MIN)}$, the high level output, source current	STRENGTH = 0 STRENGTH = 1 STRENGTH = 2 STRENGTH = 3	–	–	4.5 9 13.5 18	mA
I_{OL}	When $V_{OL} = V_{OL(MAX)}$, the low level output, sink current	STRENGTH = 0 STRENGTH = 1 STRENGTH = 2 STRENGTH = 3	–	–	4.5 9 13.5 18	mA
I_{IL}	Low input current (Pin pull up and pull down are disabled)	V_{DVDD} = 3.3V V_{IH} = 0 V	–	–	2	uA
I_{IH}	High level input current (Pin pull up and pull down are disabled)	V_{DVDD} = 3.3V $V_{IH} = V_{DVDD}$	–	–	2	uA
$\sum I_{OH}$	sum of output source current for each I/O group [1]	–	–	–	80	mA
$\sum I_{OL}$	sum of input sink current for each I/O group [1]	–	–	–	80	mA
R_{PU}	Input pull-up resistor	–	–	41	–	kΩ
R_{PD}	Input pull-down resistor	–	–	42	–	kΩ

5.4 Buck DC-DC Power Supply Characteristics

Table 5-4: Buck DC-DC Power Supply Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{th1(VDDGUV)}$	VDDG undervoltage trigger threshold	–	–	5.4	–	V
$V_{th0(VDDGUV)}$	VDDG undervoltage relief threshold	–	–	5.9	–	V
V_{SW_DCDC}	DC/DC output voltage	–	3.15	3.3	3.45	V
$R_{DSON(HS)}$	DC/DC high side conduction resistance value	–	–	1.78	–	Ω
$R_{DSON(LS)}$	DC/DC low edge conduction resistance values	–	–	0.576	–	Ω
η	Efficiency	200mA@V_{VDDG} = 15V	–	83	–	%
I_{clamp}	Current limiting threshold	–	–	400	–	mA

Figure 5-1: Switching power efficiency (T_A = 25 °C)

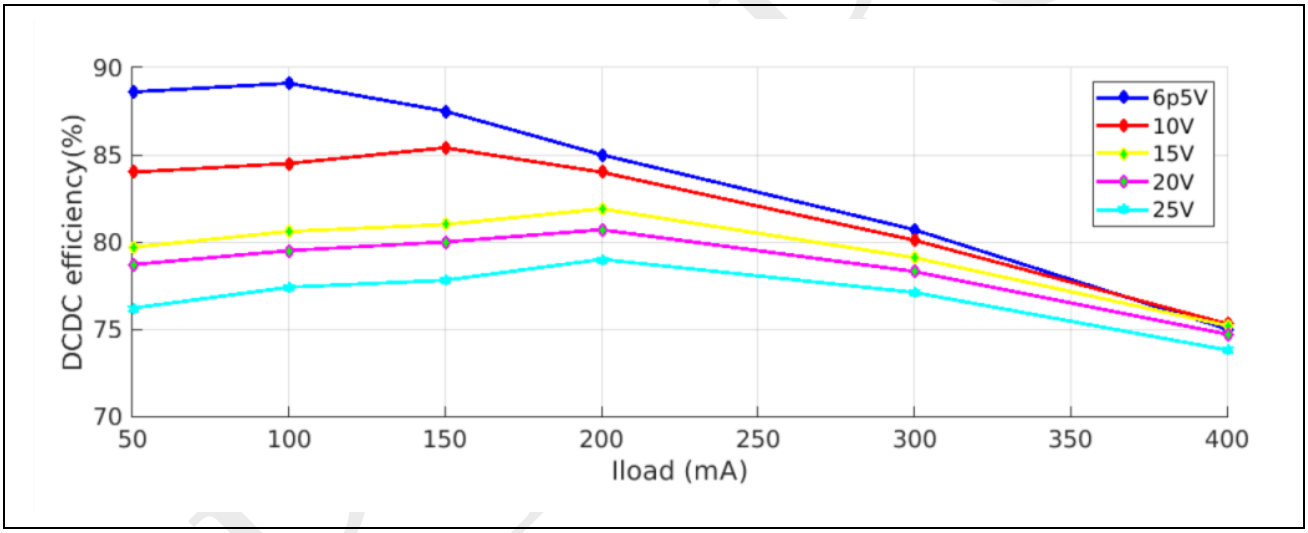
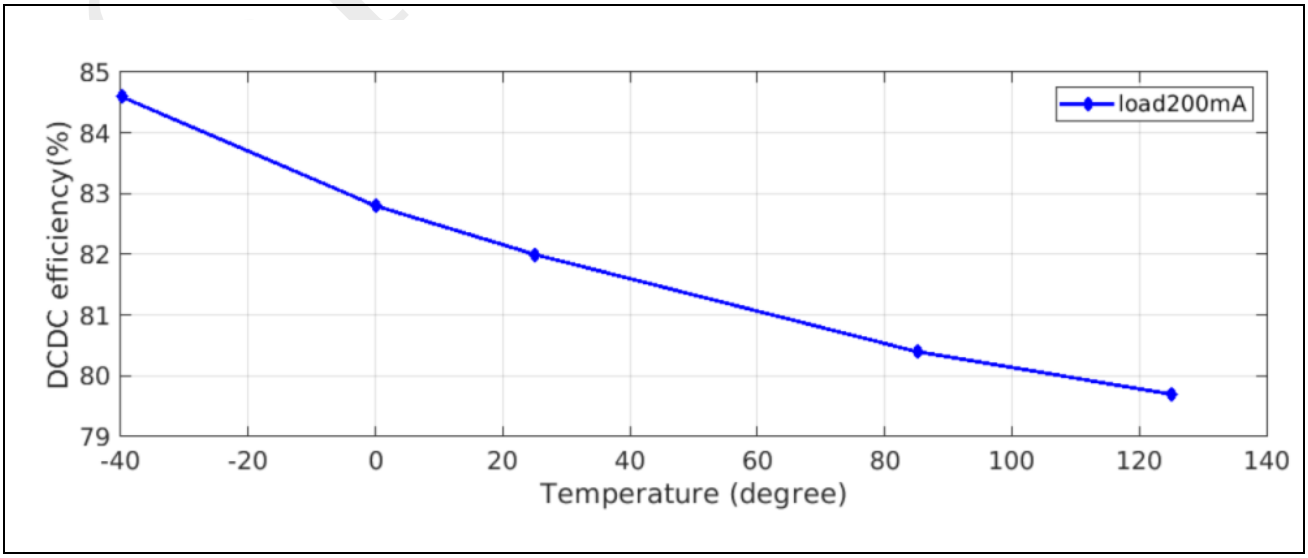


Figure 5-2: Switching power efficiency as a function of temperature (DVDD load current of 200mA)



5.5 Power consumption

Typical current consumption

In working mode, SPD1121 is in the following states:

- All input/output pins are in input mode and remain disconnected;
- All peripherals (including analog modules) are enabled;
- All peripheral clocks are as fast as HCLK (split at 1) except SPI (Max 62.5MHz), I2C (Max 62.5MHz), and DGCLK (Max 62.5MHz);
- All clock modules are enabled;
- The system clock source is the PLL clock.

In sleep mode, SPD1121 is in the following states:

- All input/output pins are in input mode and remain disconnected;
- All peripherals (including analog modules) have no clock input or are disabled;
- Clock modules (PLL, RCO1 and XO) are disabled;
- The 1.2V LDO is turned off to 0V.

The typical current consumption of SPD1121 measured from a 15V DVDD is shown in Table 5-5.

Table 5-5: SPD1121 Typical Current Consumption (running in FLASH)

Mode	Conditions		Typ.		Unit
	f_{CPU}	f_{pll}	RCO as clock source	XO as clock source	
Operation	125MHz	125MHz	14.54	16.78	mA
	100MHz	100MHz	14.11	16.33	mA
	75MHz	75MHz	13.61	15.82	mA
	50MHz	50MHz	13.06	15.27	mA
	32MHz	32MHz	12.49	14.66	mA
Sleep	–	–	1.94		mA

[1] The measurement conditions for typical values are T_A = 25 °C, VDDG = 15 V.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is shown in Table 5-6. The MCU is in the following state:

- All input/output pins are in input mode and remain disconnected;
- All peripherals (including analog peripherals, RCO and XO) are disabled without further explanation;
- The given value is calculated from the measured current consumption;
- All peripheral clocks are disabled;
- Only one peripheral is enabled;

Table 5-6: Peripheral current consumption

Peripheral [1]	Conditions	Typ[2]	Unit
BOD	RCO is the system clock source. All other peripherals are in the default state.	11	uA
ADC	PLL clock is the system clock source. All peripheral clocks are as fast as HCLK. f_{HCLK} = 125 MHz and f_{PLL} = 125 MHz	2.577	mA
T-sensor		104	uA
DPGA[3]		644	uA
ADC		163	uA
COMP		154	uA
UART	The UART clock is 125MHz and 38400 bps	93	uA
I2C	The I2C clock is 62.5MHz and 2Mbps	98	uA
SPI	The SPI clock is 62.5MHz at 30Mbps	27	uA
PWM	The PWM clock is 125MHz	288	uA
ECAP	The ECAP clock is 125MHz	26	uA
WDT	The watchdog WDT clock is 125MHz	32	uA
Timer	The timer clock is 125MHz	46	uA
CRC	The CRC clock is 125MHz	6	uA
FLASH	The HCLK clock is 125MHz	1.002	mA
XO	The RCO is used as the PLL clock source, and the PLL is used as the clock source of the CPU with f_{PLL}=125MHz	744	uA
RCO	The XO is used as the PLL clock source, and the PLL is used as the clock source of the CPU with f_{PLL}=125MHZ	30	uA
PLL	The RCO acts as the clock source for the CPU with f_{PLL}=125MHz	180	uA

[1] When the peripheral has more than one module, the above current value is the consumption of all modules. For example, the PWM current value of 288uA represents the total consumption of all the PWM modules.

[2] The measurement conditions for typical values are T_A = 25 °C, DVDD = 15 V.

[3] The DPGA module includes the consumption of the D2S buffer when tested.

5.6 Internal 1.2V regulator characteristics

Table 5-7: Internal 1.2V regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
V_{VCAP12}	Output voltage	No load	–	1.22	–	V
$I_{load(max)}$	Maximum load	–	–	–	70	mA
ΔV_{VCAP12}	Load adjustment ratio	load current 70mA	–	15	30	mV
$C_{load(ext)}$	Load capacitance	–	–	2.2+0.1+0.1	–	uF
I_{clamp}	Current of clamp	Work as usual	130	170	–	mA
		Startup	–	30	–	mA
I_{on}	Current of operation	–	–	50	–	uA

5.7 BOD Characteristics

Table 5-8: BOD Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
$V_{th1(VDD33OV)}$	DVDD overvoltage trigger threshold	–	–	3.42	–	V
$V_{th0(VDD33OV)}$	DVDD overvoltage revocation threshold	–	–	3.31	–	V
$V_{th1(VDD33UV)}$	DVDD undervoltage trigger threshold	–	–	2.58	–	V
$V_{th0(VDD33UV)}$	DVDD undervoltage revocation threshold	–	–	2.65	–	V
$V_{th1(VDD12OV)}$	VCAP12 overvoltage trigger threshold	–	–	1.33	–	V
$V_{th0(VDD12OV)}$	VCAP12 overvoltage revocation threshold	–	–	1.31	–	V
$V_{th1(VDD12UV)}$	VCAP12 undervoltage trigger threshold	–	–	0.94	–	V
$V_{th0(VDD12UV)}$	VCAP12 undervoltage revocation threshold	–	–	0.97	–	V
I_{on}	Current of operation	–	–	91.2	–	uA

5.8 RCO Characteristics

Table 5-9: RCO Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
f_{RCO}	RCO frequency	T_J = 25°C	–	32	–	MHz
ACC_{RCO}	f_{RCO} accuracy (f_{RCO} variation versus temperature)	T_J = -40~125°C	-1.5	–	1.5	%
I_{on}	Current of operation	–	–	149.8	–	uA

5.9 PLL Characteristics

Table 5-10: PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
f_{VCO}	VCO frequency	–	400	–	600	MHz
f_{PFD}	Phase detector input frequency	–	4	–	8	MHz
t_{settle}	Setup time	–	–	–	15	us
I_{on}	Current of operation	–	–	440	–	uA

5.10 13-bit ADC Characteristics

Table 5-11: ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Analog supply voltage	–	2.97	3.3	3.63	V
N_R	Resolution	No missing codes (monotonic)	–	13	–	bits
t_{sample}	Sampling time	–	200	–	–	ns
$t_{convert}$	Conversion time	–	250	–	–	ns
V_{in}	Input voltage range	–	0	–	V_{DVDD}	V
V_{FS}	Full scale voltage	–	–	3.339	–	V
V_{ref}	Voltage reference	–	1.194	1.2	1.206	V
I_{on}	Current of operation	V_{DVDD}= 3.3 V	–	8	12	mA
INL	Integral linear error	–	-3.0	–	3.0	LSB
DNL	Differential linear error	–	-1.0	–	1.0	LSB
E_{offset}	Offset error [1]	Calibration at T_J= 25°C	-2	–	2	LSB
E_{gain}	Gain error [1]		-4	–	4	LSB
T_{coef}	ADC temperature coefficient based on internal reference	–	–	35	–	ppm/°C
$ENOB_{DC}$	Number of significant bits (DC input)	–	–	11.8	–	bits
SNR	Signal to noise ratio	f_{in} = 10 kHz V_{in} = 0.94 FS N = 8192 Select XO as clock source	–	72.5	–	dBFS
THD	Total harmonic distortion		–	-86.9	–	dBFS
ENOB	Number of significant bits		–	11.7	–	bit
SFDR	Spurious free dynamic range		–	90.4	–	dBFS
SNR	Signal to noise ratio	f_{in} = 100 kHz V_{in} = 0.94 FS N = 8192 Select XO as clock source	–	72.3	–	dBFS
THD	Total harmonic distortion		–	-88.5	–	dBFS
ENOB	Number of significant bits		–	11.8	–	bit
SFDR	Spurious free dynamic range		–	89.2	–	dBFS
SNR	Signal to noise ratio	f_{in} = 10 kHz V_{in} = 0.94 FS N = 8192 Select RCO as clock source	–	65.7	–	dBFS
THD	Total harmonic distortion		–	-90.6	–	dBFS
ENOB	Number of significant bits		–	10.6	–	bit
SFDR	Spurious free dynamic range		–	69.5	–	dBFS
SNR	Signal to noise ratio	f_{in} = 100 kHz V_{in} = 0.94 FS N = 8192 Select RCO as clock source	–	66.2	–	dBFS
THD	Total harmonic distortion		–	-88.2	–	dBFS
ENOB	Number of significant bits		–	10.65	–	bit
SFDR	Spurious free dynamic range		–	70.97	–	dBFS

[1] Design-verified parameter (not production-tested).

[2] The offset and gain can be automatically calibrated by hardware.

5.11 DPGA Characteristics

Table 5-12: DPGA Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{in}	Differential input voltage range	–	-2.7/G	–	+2.7/G	V
V_{out}	Output voltage range	–	0.3	–	V_{DVDD}-0.3	V
R_{in}	Input impedance	–	–	4	–	kΩ
G	Gain	Differential mode	2/4/8/16/24/32/48/64			-
E_{gain}	Error of gain	Differential gain = 2	-1.5	–	1.5	%
		Differential gain = 16	-1	–	1	%
		Differential gain = 64	-1	–	1	%
V_{offset}	Offset	Differential gain = 2	-3	–	9	mV
		Differential gain = 16	-2	–	4	mV
		Differential gain = 64	-2	–	4	mV
V_{CM}	Common mode input voltage range	Differential gain = 2	-1.5	–	2	V
		Differential gain = 4	-0.9	–	2	V
		Differential gain = 8	-0.75	–	2	V
		Differential gain = 16	-0.6	–	2	V
		Differential gain = 24	-0.57	–	2	V
		Differential gain = 32	-0.55	–	2	V
		Differential gain = 48	-0.52	–	2	V
		Differential gain = 64	-0.5	–	2	V
t_{settle}	Settle time[1]	Differential gain = 2	–	313.7	441.6	ns
		Differential gain = 4	–	303.1	425.5	ns
		Differential gain = 8	–	268.4	423.8	ns
		Differential gain = 16	–	376.7	604.7	ns
		Differential gain = 24	–	355.8	598.9	ns
		Differential gain = 32	–	442.9	742.3	ns
		Differential gain = 48	–	628.0	1061.0	ns
		Differential gain = 64	–	813.3	1378.0	ns
GBW	Gain bandwidth [2]	Differential gain = 2	6	9.68	–	MHz
		Differential gain = 4	3.8	6.07	–	MHz
		Differential gain = 8	2.56	3.45	–	MHz
		Differential gain = 16	1.37	1.85	–	MHz
		Differential gain = 24	1.23	1.63	–	MHz
		Differential gain = 32	0.93	1.23	–	MHz
		Differential gain = 48	0.63	0.83	–	MHz
		Differential gain = 64	0.4	0.63	–	MHz
SR	Swing rate [3]	Differential gain = 2	15	21	30	V/us
		Differential gain = 4	15	21	30	V/us
		Differential gain = 8	14.5	21	30	V/us
		Differential gain = 16	11.2	18.9	29.7	V/us
		Differential gain = 24	12.57	21	33.4	V/us
		Differential gain = 32	9.25	18.4	31.8	V/us
		Differential gain = 48	6.1	11.5	25	V/us

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Differential gain = 64	4.6	8.6	17.6	V/us
$ENOB_{DC}$	Number of significant bits (DC input)	Differential gain = 2	–	11.93	–	bits
		Differential gain = 16	–	11.57	–	bits
		Differential gain = 64	–	10.94	–	bits
SNR	Signal to noise ratio f_{in} = 10kHz	Differential gain = 2	–	72.2	–	dBFS
		Differential gain = 16	–	71.1	–	dBFS
		Differential gain = 64	–	64.8	–	dBFS
THD	Total harmonic distortion f_{in} = 10kHz	Differential gain = 2	–	79.59	–	dBFS
		Differential gain = 16	–	81.29	–	dBFS
		Differential gain = 64	–	78.47	–	dBFS
$CMRR_{DC}$	Common Mode Rejection Ratio (DC input)	Differential gain = 2	–	-59.7	–	dBFS
		Differential gain = 16	–	-52.6	–	dBFS
		Differential gain = 64	–	-61	–	dBFS
$PSRR_{DC}$	Power rejection ratio (DC input)	Differential gain = 2	–	-72.8	–	dBFS
		Differential gain = 16	–	-84.9	–	dBFS
		Differential gain = 64	–	-93.4	–	dBFS
I_{on}	Current consumption	Differential gain = 2	–	1.215	–	mA
		Differential gain = 16	–	1.096	–	mA
		Differential gain = 64	–	1.152	–	mA

[1] Setup time refers to the time when the step input to output is set up to 98%. The corresponding differential output is from -2.7V to 2.7V (VDVDD = 3.3V). This index is guaranteed by design.

[2] GBW data is guaranteed by design.

[3] SR data refers to the output signal from 10% to 90% of the swing rate, guaranteed by the design.

Figure 5-3: Settle time versus Gain relationship (DPGA)

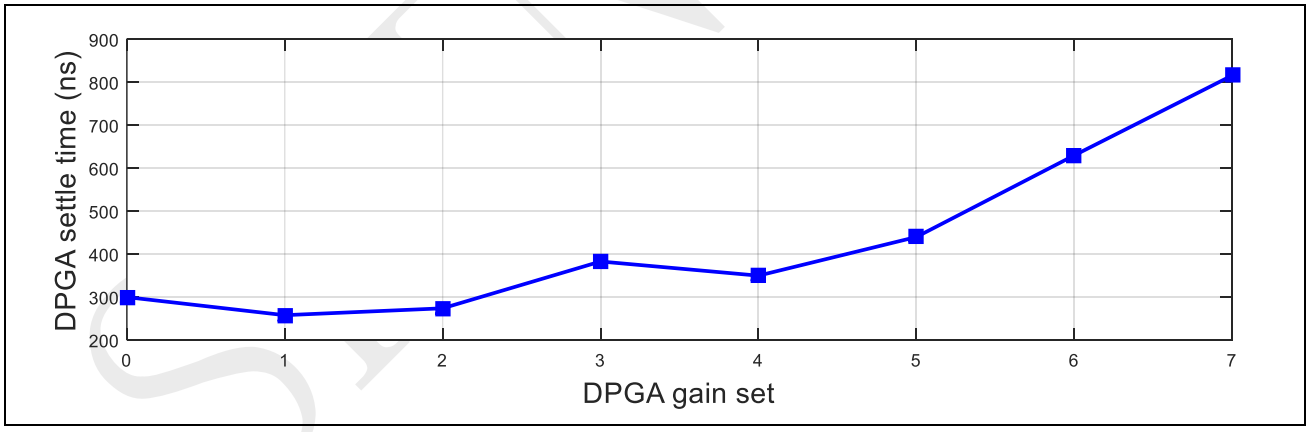


Figure 5-4: $ENOB_{DC}$ versus Gain relationship (DPGA)

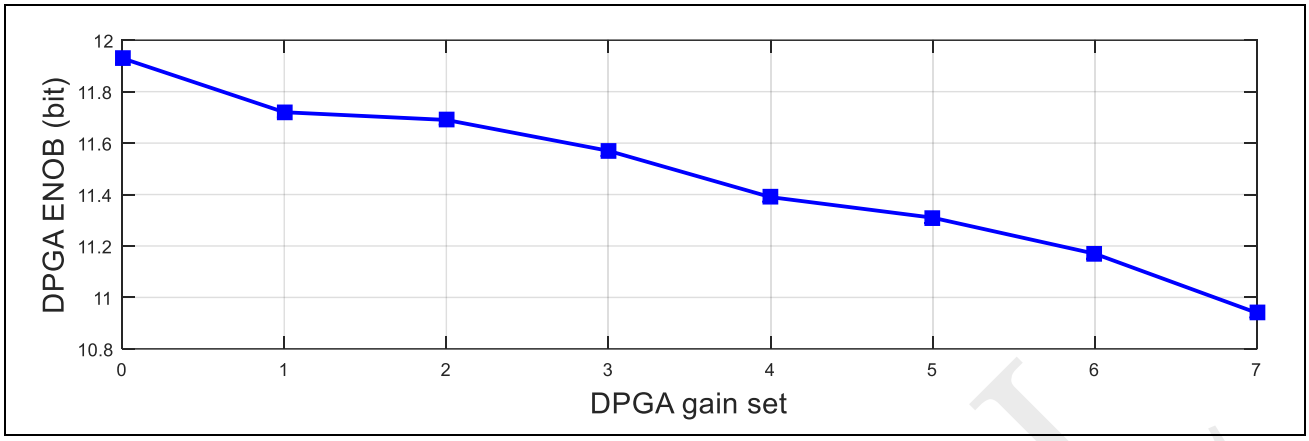


Figure 5-5: SNR versus Gain relationship (DPGA)

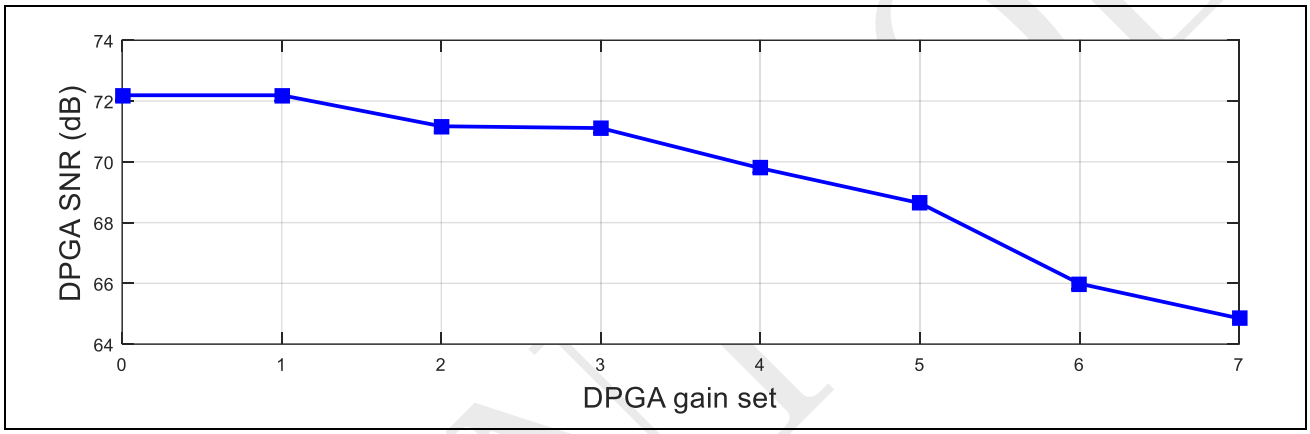


Figure 5-6: THD versus Gain relationship (DPGA)

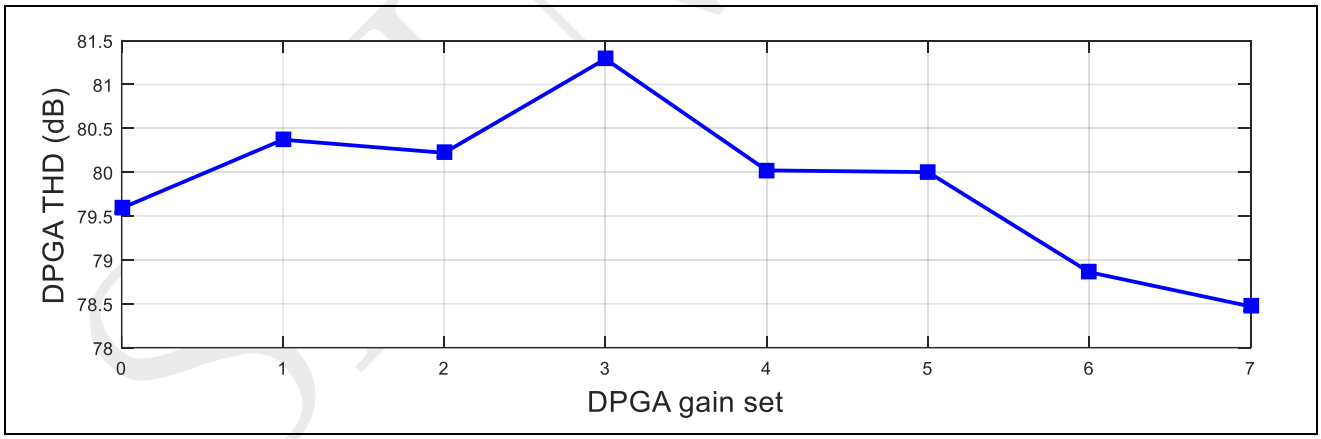


Figure 5-7: $CMRR_{DC}$ versus Gain relationship (DPGA)

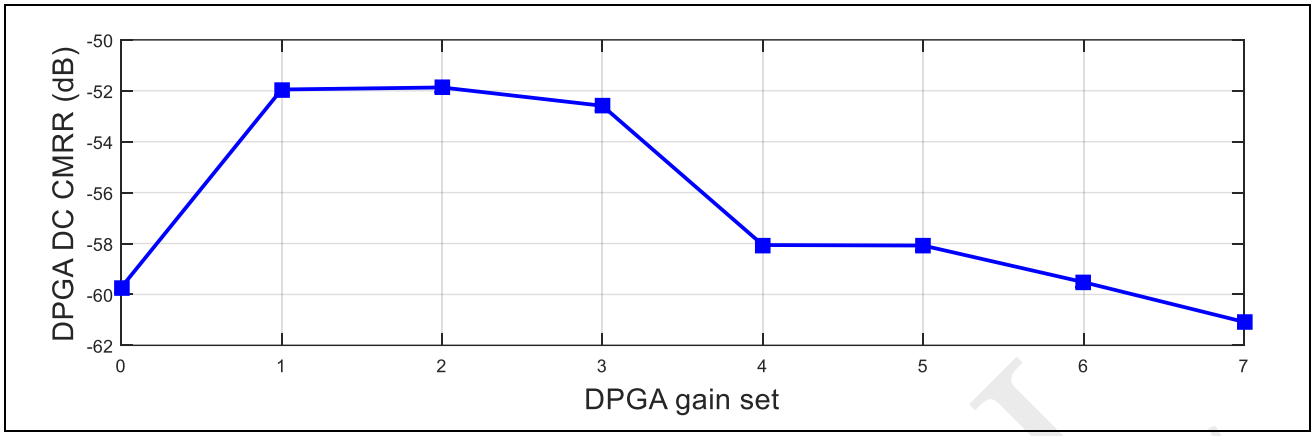
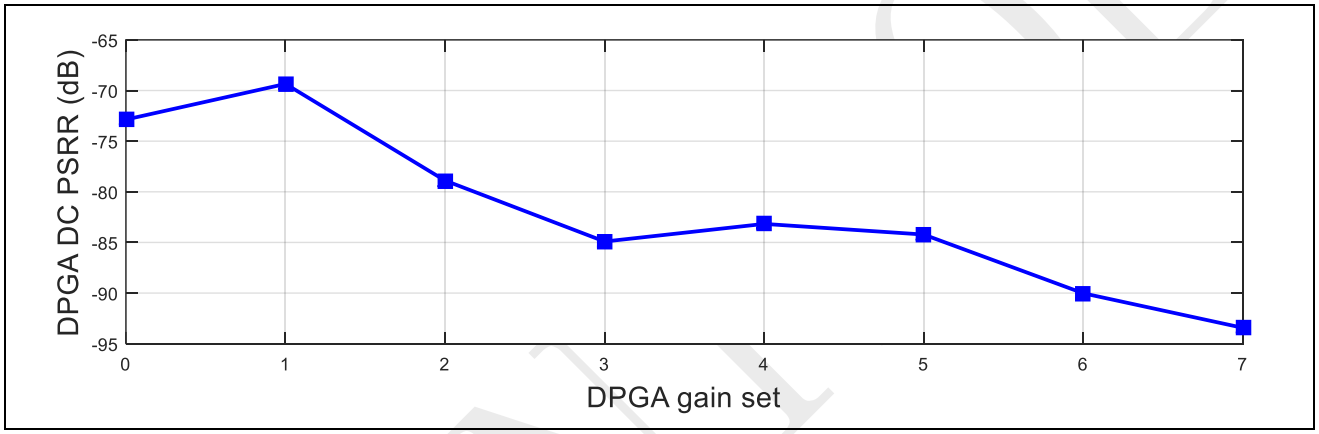


Figure 5-8: $PSRR_{DC}$ versus Gain relationship (DPGA)



5.12 D2S buffer Characteristics

Table 5-13: D2S buffer Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
V_{out}	Output voltage range	–	0.3	–	V_{DVDD} - 0.3	V
t_{settle}	Settle time [1]	–	–	10	–	ms
E_{offset}	Error of offset	–	–	10	–	mV
E_{gain}	Error of gain	–	–	1	–	%
C_L	Capacitive load	–	–	1	–	uF
I_{on}	Current consumption	–	–	1.14	–	mA

[1] The settle time is measured by adding an external RC filter circuit, and typical values are: R = 1kΩ, C = 1uF.

5.13 T-sensor Characteristics

Table 5-14: Tsensor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	3.3V supply voltage	–	2.97	3.3	3.63	V
T_{slope}	Resolution	13-bit ADC converted to full amplitude 3.339V	–	–	1.74	°C/LSB
E_T	Error of temperature	-40°C ~ +125°C	-12	–	12	°C
T_{stup}	Startup time	–	–	4.00	–	us
T_{acq}	Time of capture	–	–	0.62	–	us
I_{on}	Current of operation	–	–	97.67	–	uA

5.14 COMP Characteristics

Table 5-15: COMP Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
V_{in}	Input voltage range	–	0	–	V_{DVDD}	V
V_{offset}[1]	Offset voltage (hysteresis voltage gear 0)	V_{DVDD} = 3.3V T_J = 25°C 1.65V commom-mode input	-10	–	–	mV
V_{hyst}	Hysteresis voltage gear 0		–	0	–	mV
	Hysteresis voltage gear 1		–	13	–	mV
	Hysteresis voltage gear 2		–	25	–	mV
	Hysteresis voltage gear 3		–	37	–	mV
t_d	Delay time From comparator reaction to PWM asynchronous shutdown (hysteresis voltage gear 0)		–	50	–	ns
I_{on}	Current of operation	–	–	59.4	–	uA

[1] Design-verified parameter (not production-tested).

5.15 Internal 10-bit DAC Characteristics

Table 5-16: DAC Characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DVDD}	Supply voltage	–	2.97	3.3	3.63	V
N	resolution	monotonic	–	10	–	bit
V_{FS}	Full scale value	–	0	–	V_{DVDD}	V
DNL[2]	Differential nonlinear error	–	-0.5	–	0.5	LSB
INL[2]	Integral nonlinear error	–	-1	–	1	LSB
E_{offset}[2]	Error of offset	–	-10	–	10	mV
t_{settle}[2]	DAC setup time	–	–	–	1	us
I_{on}	Current of operation	–	–	96.3	–	uA

[1] The DAC generates a static voltage as the threshold of the comparator and does not guarantee the performance of dynamically changing the code value to generate the waveform.

[2] Design-verified parameter (not production-tested).

5.16 Flash Characteristics

Table 5-17: Flash Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max
t_{read}	Read operation time	–	48	–	ns
$t_{prog,enter}$	Programming mode entry time	–	24	–	us
$t_{preprog}$	Word (32-bit) pre-programming time	–	2.5	3.5	us
$t_{preprog,exit}$	Pre-programming mode exit time	–	10	–	us
t_{prog}	Word (32-bit) programming time	–	8	10	us
$t_{prog,exit}$	Programming mode exit time	–	5.1	–	us
t_{SE}	Sector erasure time	–	3.2	4	ms
t_{BE}	Block erase time	–	4	6	ms
t_{CE}	Overall erasure time	–	8	10	ms
N_{cycle}	Number of erasable writes	T_J = 85 °C	–	100,000	cycles
$t_{retention}$	Data retention period	T_J = 85 °C	–	10	years

5.17 SPI Characteristics

Figure 5-9: SPI host mode interface timing diagram

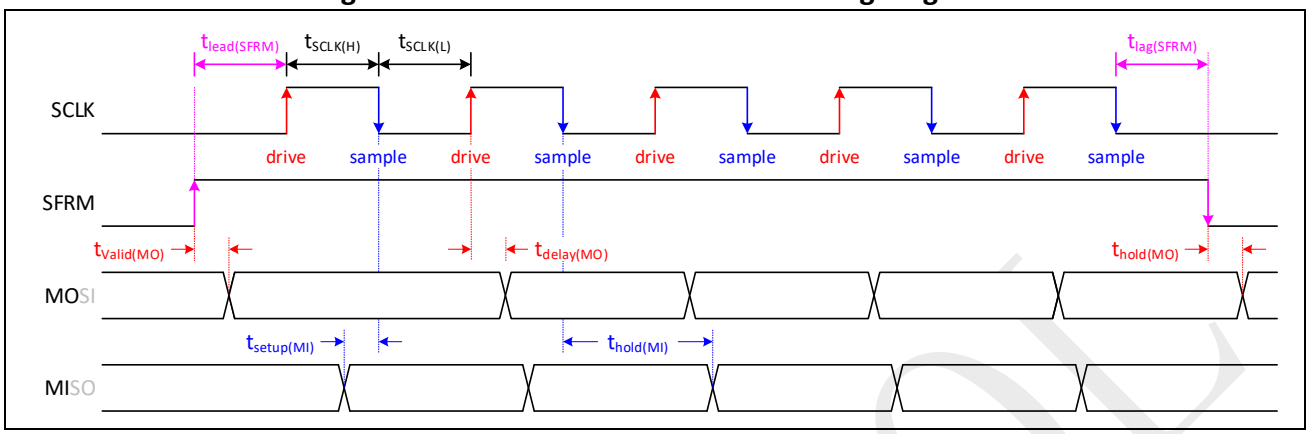


Table 5-18: Timing characteristics of SPI host mode interface[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	15pF pin capacitance	–	–	30	MHz
$t_{SCLK(H)}$	SCLK high level time		16.6	–	–	ns
$t_{SCLK(L)}$	SCLK low time		16.6	–	–	ns
$t_{lead(SFRM)}$	The time of the SFRM effective edge leading the first SCLK clock edge		$t_{SCLK}/2 – 5.5$	–	$t_{SCLK}/2 – 2.1$	ns
$t_{lag(SFRM)}$	The time of the SFRM invalid edge to lag the last SCLK clock edge		$t_{SCLK}/2 – 2.3$	–	$t_{SCLK}/2 – 1$	ns
$t_{valid}(MO)$	SFRM effectively along the delay to MOSI flip		2.5	–	6.8	ns
$t_{hold}(MO)$	The delay from the SFRM invalidation to the MOSI flip		2.5	–	7.2	ns
$t_{delay}(MO)$	The SCLK drives the delay along to the MOSI flip		3	–	8.1	ns
$t_{setup}(MI)$	Establishment time of MISO to SCLK sampling edge		15	–	–	ns
$t_{hold}(MI)$	Holding time from MISO to SCLK sampling edge		-2.5	–	–	ns

[1] Design-verified parameter (not production-tested).

Figure 5-10: SPI slave mode interface timing diagram

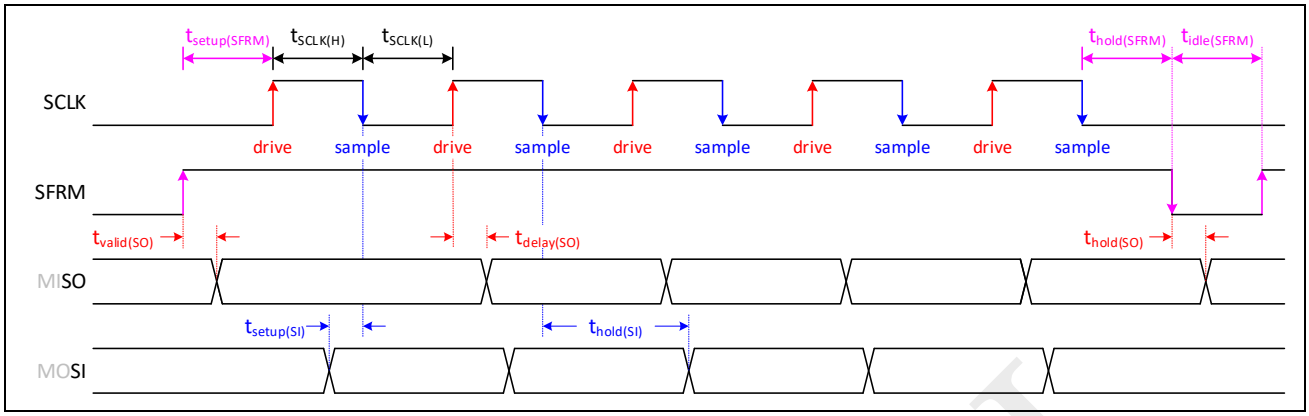


Table 5-19: SPI Timing Characteristics of Slave Mode interface [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	15pF pin capacitance	–	–	30	MHz
$t_{SCLK(H)}$	SCLK high level time		16.6	–	–	ns
$t_{SCLK(L)}$	SCLK low time		16.6	–	–	ns
$t_{idle(SFRM)}$	The time during which the SFRM remains invalid between adjacent frames		4 x t_{CLK_CPU}	–	–	ns
$t_{setup(SFRM)}$	The first SCLK clock is valid along the establishment time of the previous SFRM		6.5	–	–	ns
$t_{hold(SFRM)}$	The last SCLK clock maintains an effective holding time along the back SFRM		2.5	–	–	ns
t_{valid}(SO)	SFRM effectively along the delay to MISO flip		6	–	15.5	ns
t_{hold}(SO)	The delay from the SFRM invalidation to the MISO flip		6	–	14.8	ns
t_{delay}(SO)	The SCLK drives the delay along to the MISO flip		6.5	–	15.3	ns
t_{setup}(SI)	Establishment time of MOSI to SCLK sampling edge		4.6	–	–	ns
t_{hold}(SI)	Holding time from MOSI to SCLK sampling edge		2.6	–	–	ns

[1] Design-verified parameter (not production-tested).

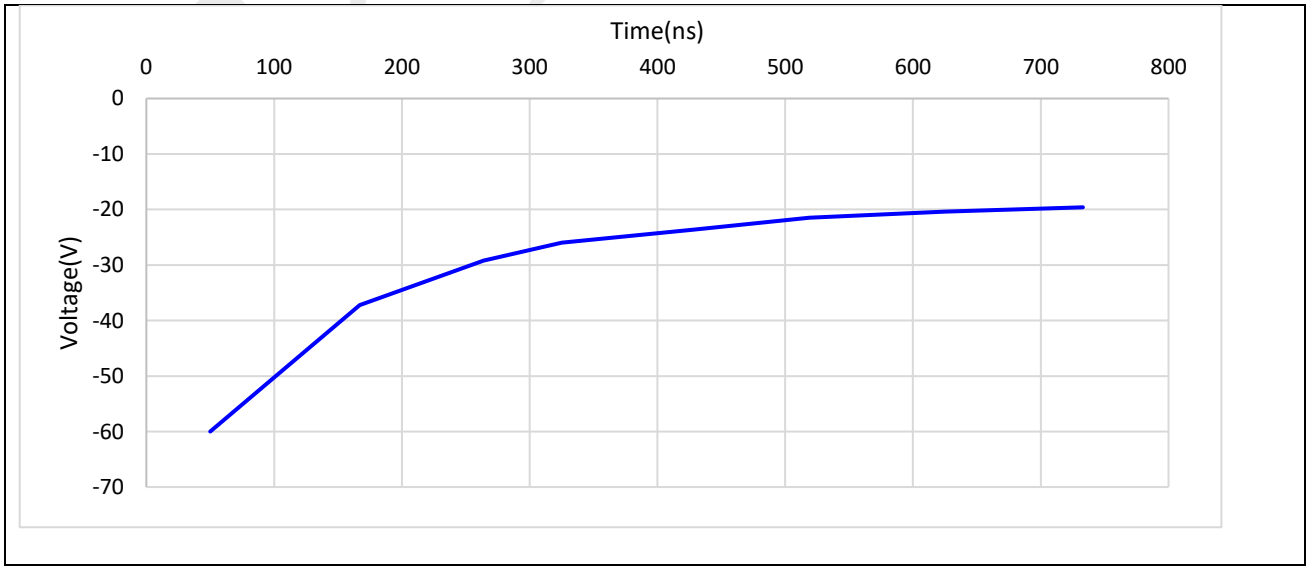
5.18 Pre-driver Characteristics

Table 5-20: Pre-driver Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{th0(VDDGUV)}$	VDDG undervoltage relief threshold	–	–	9.6	–	V
$V_{th1(VDDGUV)}$	VDDG undervoltage trigger threshold	–	–	8.9	–	V
$V_{hyst(VDDGUV)}$	VDDG undervoltage hysteresis	–	–	0.7	–	V
$V_{th0(VBSUV)}$	Upper tube power rail (VBOOT-VPX) undervoltage relief threshold	–	–	9.6	–	V
$V_{th1(VBSUV)}$	Upper tube power rail (VBOOT-VPX) undervoltage trigger threshold	–	–	8.9	–	V
$V_{hyst(VBSUV)}$	Undervoltage hysteresis of upper tube power rail (VBOOT-VPX)	–	–	0.7	–	V
$I_{leakage(VBS)}$	VBOOT leakage current	V_{BS} = 600V V_{HS} = 600V	–	1	–	uA
$I_{Q(HS)}$	Upper tube power rail static current	–	–	36	100	uA
I_{PU}	Pull up drive current	–	–	200	–	mA
I_{DN}	Pull down drive current	–	–	350	–	mA
t_{FILT_IN}	GPIO input signal filtering time	–	–	250	–	ns
t_{on}[1]	Turn-on transmission delay	–	–	425	–	ns
t_{off}[1]	Turn off transmission delay	–	–	400	–	ns
t_D[1]	Dead time	–	–	400	–	ns
t_M[1]	The open/close delay mismatch between the six channels	–	–	13	75	ns
t_{MD}[1]	On/off delay mismatch max(t_{ON}, t_{OFF}) - min(t_{ON}, t_{OFF})	–	–	13	75	ns

[1] Delay and leakage variations cover the temperature range of -40°C to 150°C.

Figure 5-11: Transient Negative Voltage



5.19 Electrical sensitivity characteristics

Table 5-21: ESD absolute maximum ratings

Symbol	Parameter	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human Body Model)	Ambient temperature T_A = 25 °C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (Charge Device Model)	Ambient temperature T_A = 25 °C	1000	V

Table 5-22: Electrical sensitivities

Symbol	Parameter	Conditions	Max	Unit
LU	Static latch-up	T_A = 125 °C, V_{CAP12} = 1.42V, V_{DVDD}=3.63V $V_{BS\_W/U/V}$ = 25V, V_{VDDG} = 25V	200	mA

5.20 Moisture Sensitivity Level characteristics

Table 5-23: Moisture Sensitivity Level characteristic

Symbol	Parameter	Conditions	Max	Unit
MSL	Moisture Sensitivity Level	–	3	–

5.21 Thermal resistance characteristics

Table 5-24: Thermal resistance characteristics (QFN38 package)

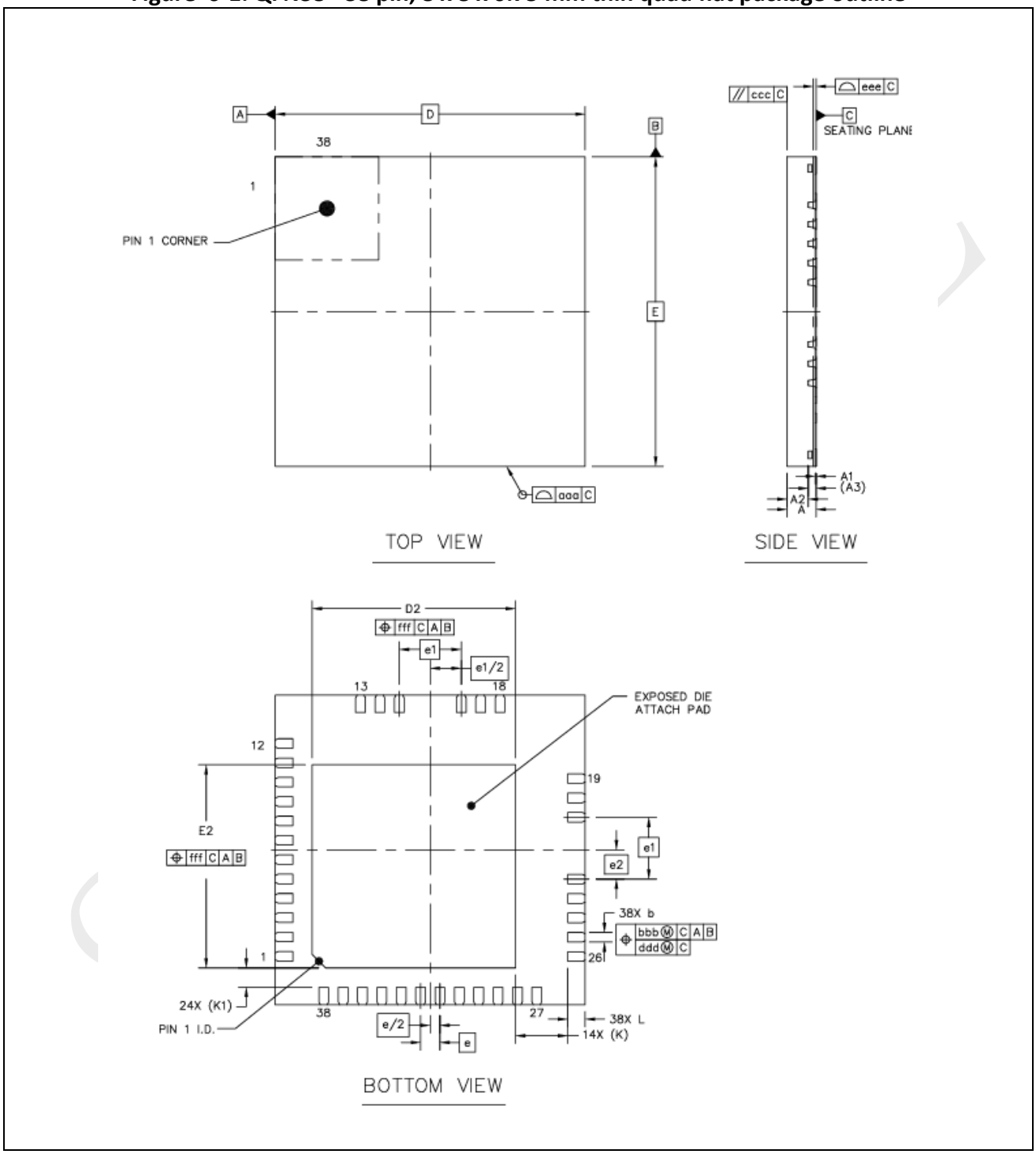
Symbol	Parameter	Conditions	Typ.	Unit
θ_{JC}	Junction-to-case thermal resistance	–	13.47	°C/W
θ_{JA}	Junction-to-ambient thermal resistance	Single layer PCB PCB Copper content = 20%	66.13	°C/W
		4-layer PCB PCB Copper content (Top layer= 20%, 2nd/3rd layer= 100%, Bottom layer = 5%)	39.90	°C/W

[1] The size of PCB test board is 76.2mm x 114.3mm x 1.6mm.

6 Package information

6.1 QFN38

Figure 6-1: QFN38 - 38 pin, 8 x 8 x 0.75 mm thin quad flat package outline

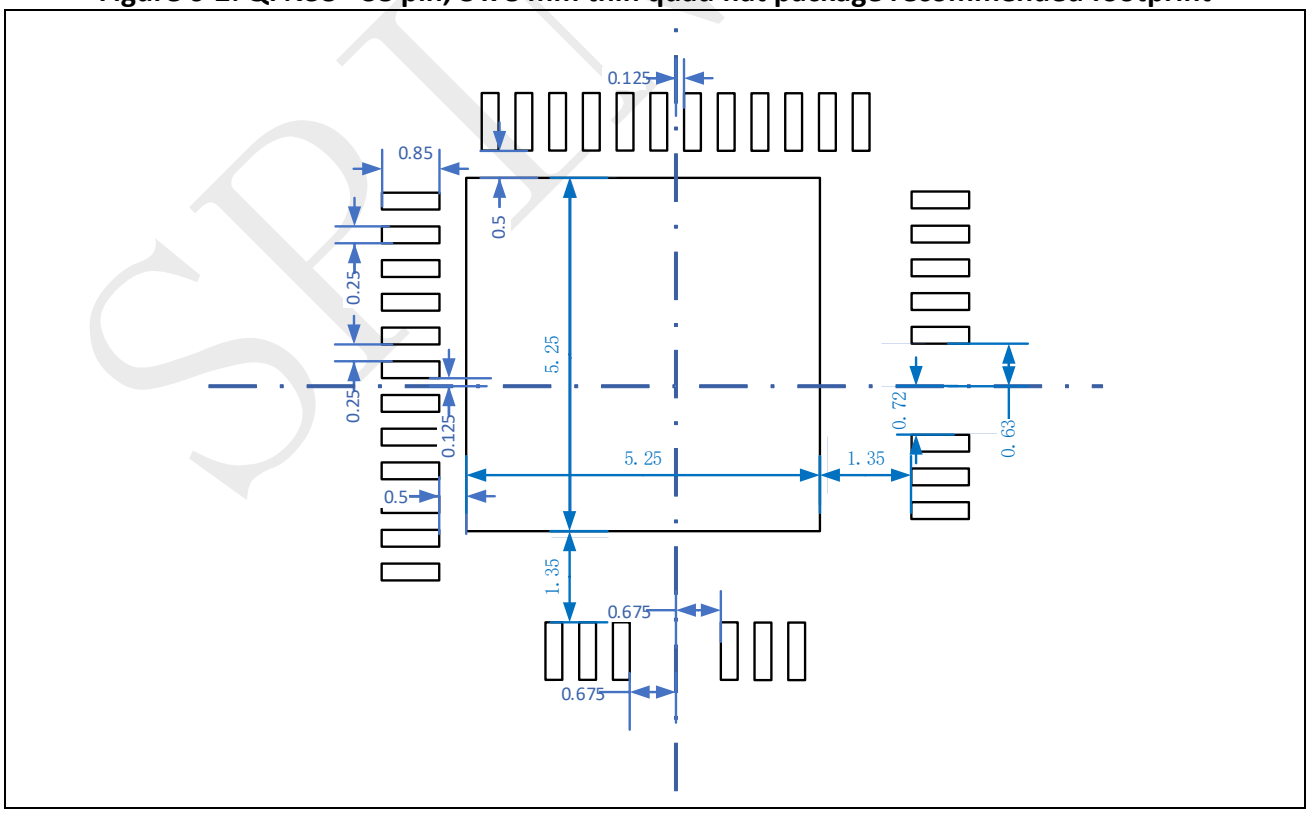


[1] Drawing is not to scale.

Table 6-1: QFN38 - 38 pin, 8 x 8 x 0.75 mm thin quad flat package mechanical data

Symbol	Unit: mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A2	–	0.55	–
A3	0.203 REF		
b	0.20	0.25	0.30
D	8 BSC		
E	8 BSC		
e	0.5 BSC		
e1	1.6 BSC		
e2	0.755 BSC		
D2	5.15	5.25	5.35
E2	5.15	5.25	5.35
L	0.35	0.45	0.55
K	1.35 REF		
K1	0.5 REF		
aaa	0.1		
ccc	0.1		
eee	0.08		
bbb	0.1		
ddd	0.05		
fff	0.1		

Figure 6-2: QFN38 - 38 pin, 8 x 8 mm thin quad flat package recommended footprint



[1] Unit: mm

7 PCB layout and routin guidance

- DVDD is the feedback for the buck DC-DC converter. To ensure the stable operation of the control loop, it is recommended to keep the DVDD trace away from high-voltage switching traces and noise sources, such as inductors.
- The SW trace should be as short and wide as possible to minimize radiation.
- The GND trace between the DVDD capacitor and the GND pin should be as wide as possible to minimize trace impedance.
- The GND trace between the VDDG bypass capacitor and the GND pin should be as wide as possible to minimize trace impedance.
- The GND trace between the VCAP12 bypass capacitor and the GND pin should be as wide as possible to minimize trace impedance.
- For the pre-driver routing, a star grounding scheme is required. The trace between the VBOOT capacitor and the VPX pin should be as wide and short as possible to minimize trace impedance.

8 Ordering information

Table 8-1: Ordering information

Ordering Number	Flash	SRAM	Max CPU Frequency	Package	Grade	SPQ[1]	Packing
SPD1121API38	64KB	32KB	125MHz	QFN38	Industrial grade -40°C~+125°C	3480	Tray
SPD1121HAPI38	128KB	32KB	125MHz	QFN38	Industrial grade -40°C~+125°C	3480	Tray

[1] SPQ = Standard Pack Quantity.

8.1 Rule of ordering number

Figure 8-1: Rule of ordering number